MODEL	REV	CHANGE LIST
TW3A M/B	3A	First Release 31T3MB0033 (E200601-0720) 2006/1/10
	3B	E200601-5311 2006/2/8

Model / Page	TW3A M/B From	To
1	3A	
2	3A	
3	3A	
4	3A	
5	3A	
6	3A	
7	3A	
8	3A	
9	3A	
10	3A	
11	3A	
12	3A	
13	3A	
14	3A	3B
15	3A	
16	3A	
17	3A	
18	3A	
19	3A	3B
20	3A	
21	3A	
22	3A	
23	3A	3B
24	3A	
25	3A	
26	3A	3B
27	3A	3B
28	3A	
29	3A	3B
30	3A	
31	3A	
32	3A	3B
33	3A	3B
34	3A	
35	3A	3B
36	3A	3B
37	3A	
38	3A	
39	3A	
40	3A	
41	3A	3B
42	3A	
43	3A	3B
44	3A	
45	3A	
46	3A	
47	3A	
48	3A	

PROJECT : TW3A
Quanta Computer Inc.

PROJECT: TW3A	ASSY P/N:31TW3MB0033	TITLE:	DOC NO:204
APPROVED BY : Johnson Hsu	DRAWING BY : Tony Huang	VER:3B	DATE :02/08/2006 SHEET 1

TW3A- DESIGN

31TW3MB00XX

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

RUN POWER SW PG 43

AC/BATT CONNECTOR PG 40

BATT CHARGER PG 40

Yonah/Merom
31W/35W
(478 Micro-FCPGA)
PG 4,5

CPU VR PG 37

DC/DC +3VSUS +5VSUS PG43

DC/DC +3VPCU +5VPCU PG38

DC/DC +1.05V +1.5V PG37

CLOCKS ICS954206 PG 3

FSB 133MHZ

DDRII VR PG 39

DDRII-SODIMM1 PG 16,17

DDRII-SODIMM2 PG 16,17

DDRII 667mhz

DDRII 667mhz

Calistoga PM
945PM
Integraded VGA Function
1466 BGA
PG 6,7,8,9,10,11

PCI-Express 16X

nVIDIA
NV72M/MV
(64 Bit B/W)
DDRII
16M*16(128MB)
32M*16(256MB)
(Bank*4)
PG 18~21

DC/DC VGA CORE PG42

LVDS(2 Channel)

Panel Connector PG 22

TVOUT

S-Video PG 35

VGA

VGA,DVI PG 23

DMI interface

SATA - HDD PG 29

PATA - HDD PG 29

Internal ODD CD-ROM PG 29

SATA0

PATA 100

ICH7-M
652 BGA
PG 12,13,14,15

USB2.0 (P0~P7)

USB2.0 (P5)

Bluetooth PG 33

USB2.0 (P0~P1,P4)

USB2.0 I/O Ports PG 26

PCI-E, 1X

LAN 88E8038/88E8055 PG 24

Magnetics PG 25

RJ45 PG 25

PCI-E, 1X

Mini PCI-E Card
PCI Express Mini Card
PG 33

PCI-E, 1X

Express Card x1 NEW CARD PG 33

PCI Bus 33MHz

Azalia

Conexant Audio CX20549-12 PG 30

LPC

TI PC7402 PG 27

IEEE1394 CONN
3 in 1 Card reader
PG28

AUDIO Amplifier PG 31

MDC DAA CX20548-A PG 32

TPM1.2 PG 44

KBC PC87541V PG 36

X-Bus

Jack to Speaker PG 31

Audio Jacks PG 30

MODEM RJ 11 PG 32

Key Matrix PG 34

Touch Pad PG 34

Flash PG 36

Power On
- Power Input
- LPT PORT
- COM PORT
- LAN
- VGA
- Headphone
- 1394
- USB X 2

RQ6
Replicator Daughter Board
USB
PG 35

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	3A

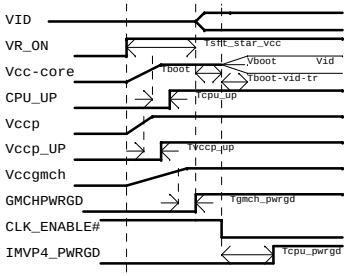
Date: Thursday, June 15, 2006 Sheet 1 of 48

Board Stack up Description

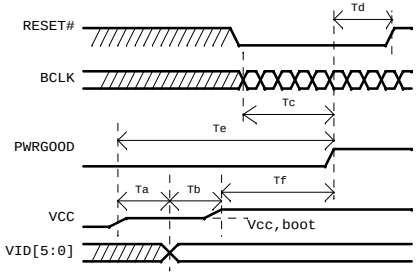
PCB Layers

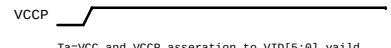
Layer 1		TOP(Component,Other)
Layer 2		Ground Plane
Layer 3		IN1
Layer 4		IN2
Layer 5		Power Plane
Layer 6		IN3
Layer 7		Ground Plane
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



Dothan Power-up Timing Specifications



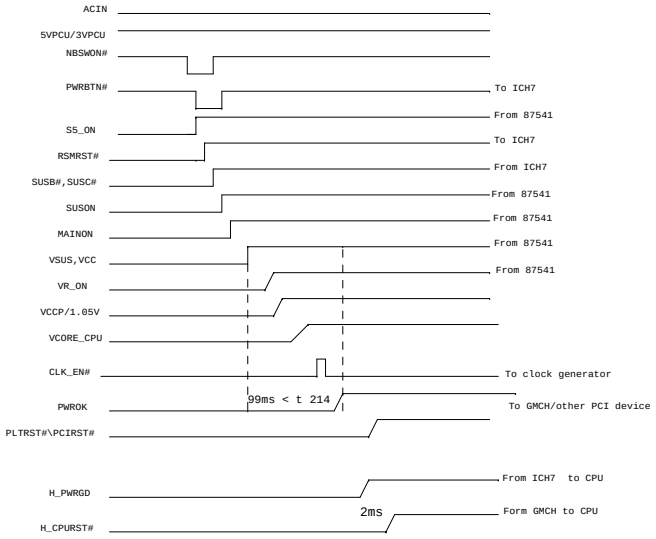


Ta=VCC and VCCP asseration to VID[5:0] vaild
Tb=VID[5:0] stable to VCC vaild
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot vaild to PWRGOOD assertion time

Voltage Rails

Voltage Rails		ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	Core voltage for Processor	X				VR_ON 0.726V~0.94V
VCCP	Core voltage for CPU / NB	X				VR_ON
SMDDR_VTERM	0.9V for DDR2 Termination voltage	X				MAINON
RVCC1.5		X	X	X		RVCC_ON
RVCC3		X	X	X		RVCCD
VCC1.5		X				MAIND
VCC2.5		X				MAINON
VCC3		X				MAIND
VCC5		X				MAIND
1.8VSUS		X	X			SUSON
3VSUS		X	X			SUSD
5VSUS		X	X			SUSD
3VPCU		X	X	X	X	VL
5VPCU		X	X	X	X	VL
9VPCU		X	X	X	X	5VPCU

ACIN POWER ON TIMING



Voltage Rails		ON S0~S1	ON S3	ON S4	ON S5	Control signal
VCC_CORE	Core voltage for Processor	X				VRON
GMCH_VTT	Core voltage for GMCH 1.05V	X				MAINON
SMDDR_VTERM	0.9V for DDR II Termination voltage	X				MAINON
SMDDR_VREF	0.9V for DDR II Reference Voltage	X				MAINON
GMCH_1.5V		X				MAINON
1.8VSUS	1.8V for DDR II voltage	X	X			SUSON
+2.5V		X				MAINON
3VPCU		X	X	X	X	VL
3VSUS		X	X			SUSON
+3V		X				MAINON
5VPCU		X	X	X	X	VL
5VSUS		X	X			SUSON
+5V		X				MAINON
VIN	POWER SOURCE	X	X	X	X	

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7402	AD17	REQ2# / GNT2#	PIRQ C/D

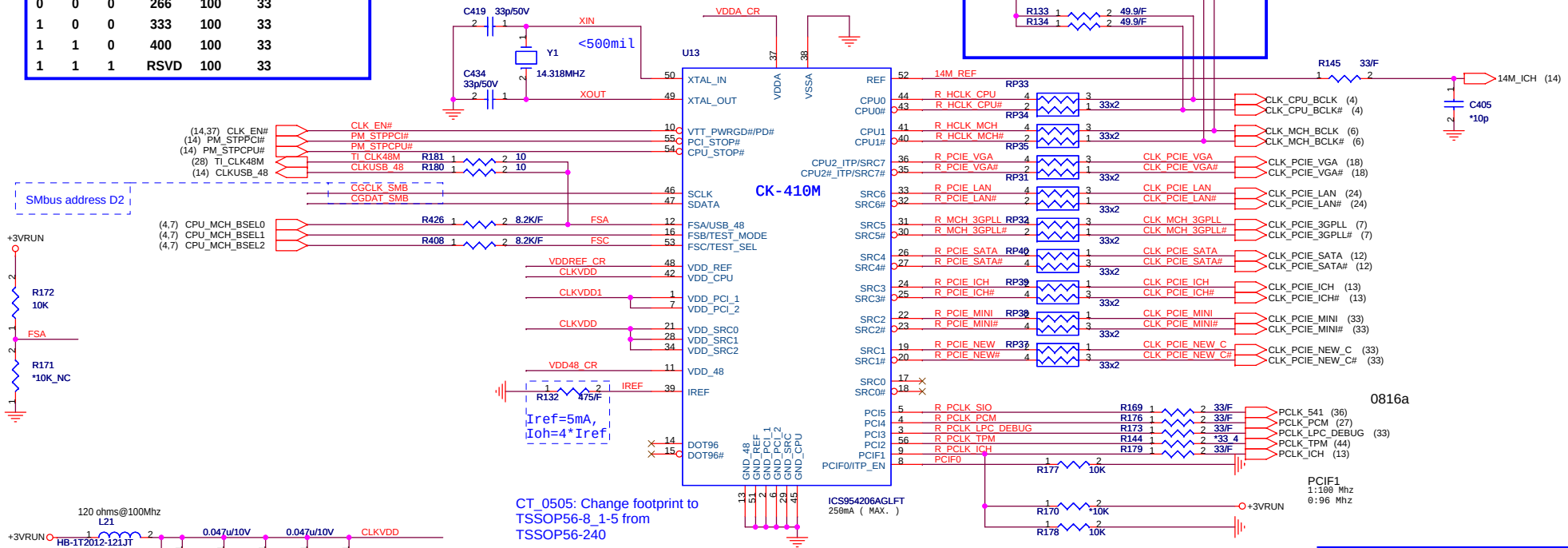
PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	System Information	3A

Date: Thursday, June 15, 2006 Sheet 2 of 48

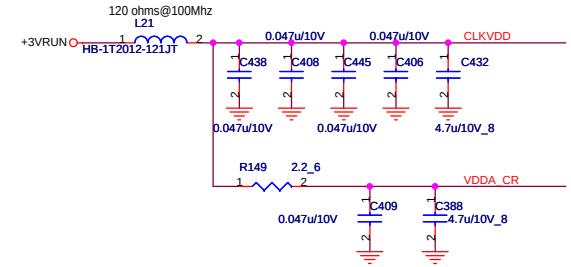
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

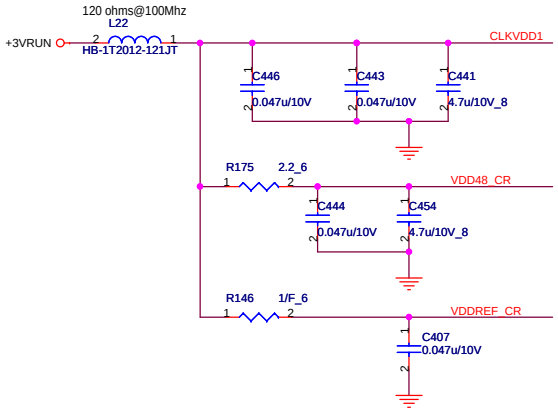
Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

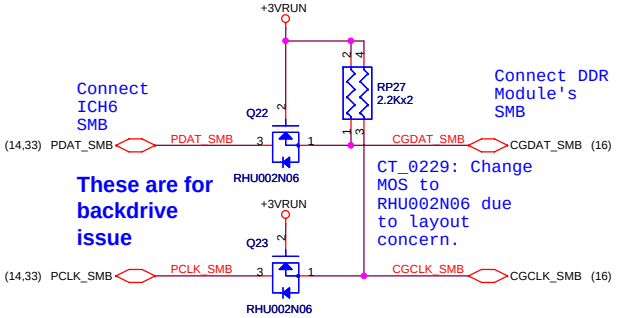


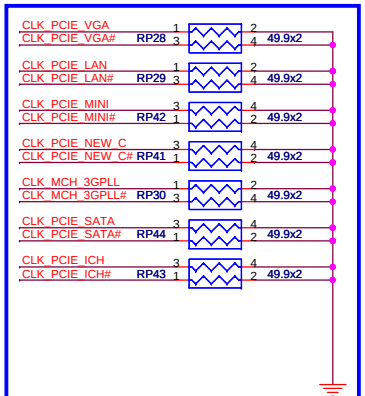
Tie to VCC (Logic 1) is for ITP using.
Tie to GND (Logic 0) is for PCIE using.

Bypass CAPs need to follow Bypass CAP. Routing Rule, no vias between CAP to CHIPSET VCC Pin or GND.









Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number	Rev
	CLOCK GENERATOR	3A
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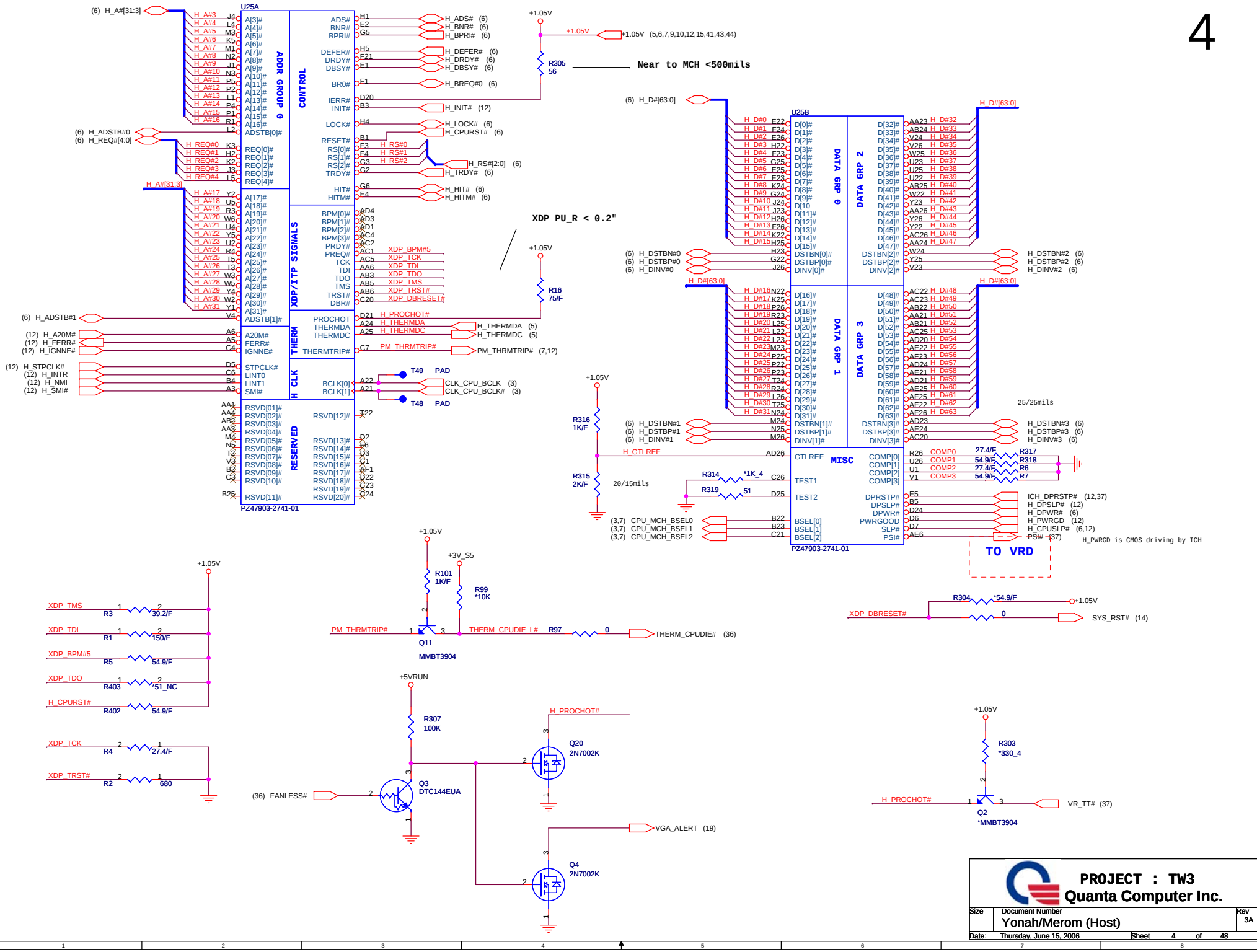
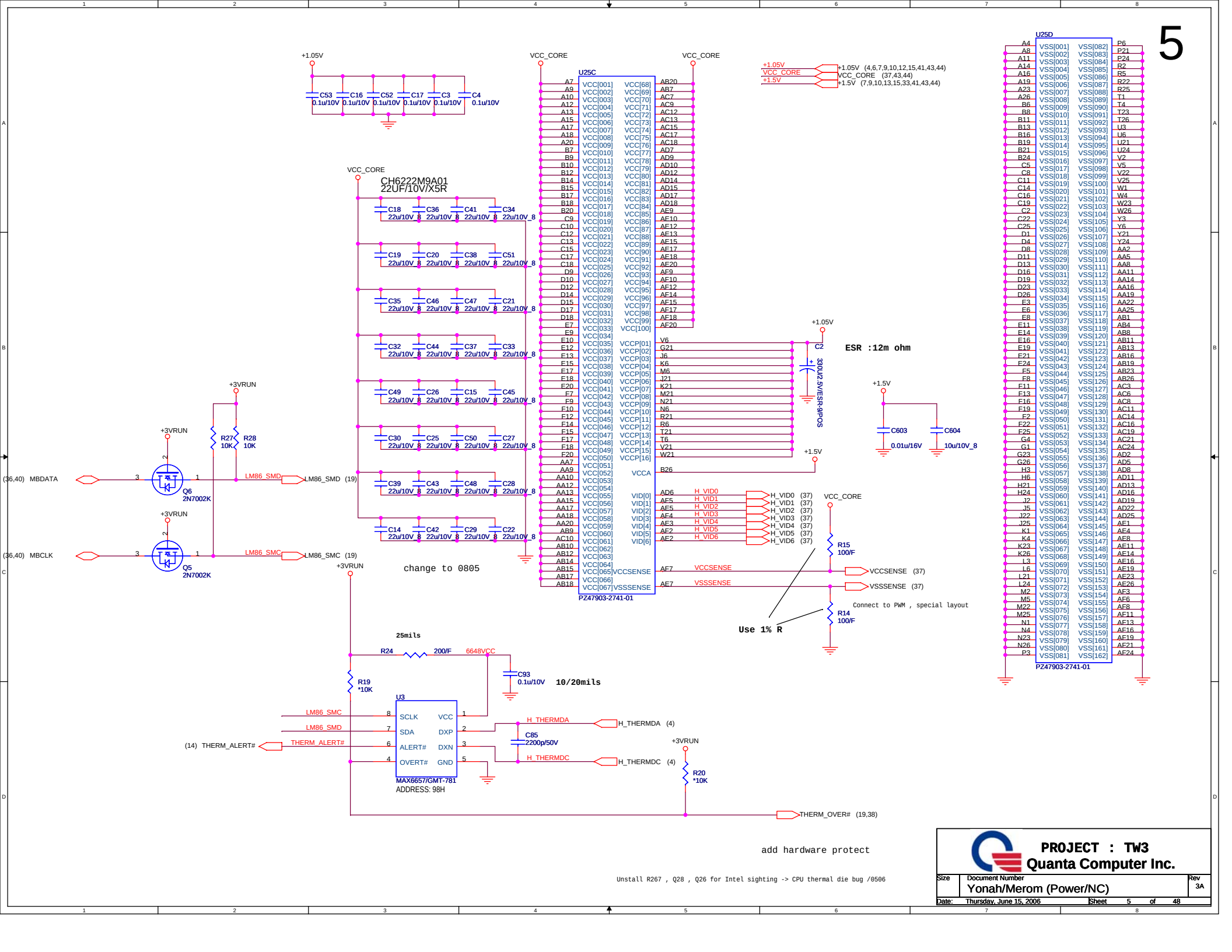

U25A
ADDR GROUP 0
CONTROL
XDP/ITP SIGNALS
THERM
H_CLK
RESERVED
PZ47903-2741-01
Near to MCH <500mils
XDP PU_R < 0.2"
U25B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
PZ47903-2741-01
TO VRD
H_PWRGD is CMOS driving by ICH
25/25mils
PROJECT : TW3
Quanta Computer Inc.
Yonah/Merom (Host)
Thursday, June 15, 2006
Sheet 4 of 48
hexainf@hotmail.com


5
+1.05V
VCC_CORE
C53 0.1u/10V
C16 0.1u/10V
C52 0.1u/10V
C17 0.1u/10V
C3 0.1u/10V
C4 0.1u/10V
U25C
PZ47903-2741-01
+1.05V (4,6,7,9,10,12,15,41,43,44)
VCC_CORE (37,43,44)
+1.5V (7,9,10,13,15,33,41,43,44)
U25D
PZ47903-2741-01
CH6222M9A01
22UF/10V/X5R
C18 22u/10V_8
C36 22u/10V_8
C41 22u/10V_8
C34 22u/10V_8
C19 22u/10V_8
C20 22u/10V_8
C38 22u/10V_8
C51 22u/10V_8
C35 22u/10V_8
C46 22u/10V_8
C47 22u/10V_8
C21 22u/10V_8
C32 22u/10V_8
C44 22u/10V_8
C37 22u/10V_8
C33 22u/10V_8
C49 22u/10V_8
C26 22u/10V_8
C15 22u/10V_8
C45 22u/10V_8
C30 22u/10V_8
C25 22u/10V_8
C50 22u/10V_8
C27 22u/10V_8
C39 22u/10V_8
C43 22u/10V_8
C48 22u/10V_8
C28 22u/10V_8
C14 22u/10V_8
C42 22u/10V_8
C29 22u/10V_8
C22 22u/10V_8
C2 330U/2.5V/ESR-9/POS
ESR :12m ohm
C603 0.01u/16V
C604 10u/10V_8
+3VRUN
R27 10K
R28 10K
(36,40) MBDATA
Q6 2N7002K
LM86_SMD
LM86_SMD (19)
(36,40) MBCLK
Q5 2N7002K
LM86_SMC
LM86_SMC (19)
change to 0805
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
R15 100/F
R14 100/F
VCCSENSE
VSSSENSE
VCCSENSE (37)
VSSSENSE (37)
Connect to PWM , special layout
Use 1% R
25mils
R24 200/F
6648VCC
C93 0.1u/10V
10/20mils
R19 *10K
U3
SCLK
SDA
ALERT#
OVERT#
VCC
DXP
DXN
GND
MAX6657/GMT-781
ADDRESS: 98H
LM86_SMC
LM86_SMD
THERM_ALERT#
(14) THERM_ALERT#
H_THERMDA
H_THERMDC
C85 2200p/50V
H_THERMDA (4)
H_THERMDC (4)
R20 *10K
THERM_OVER# (19,38)
add hardware protect
Unstall R267 , Q28 , Q26 for Intel sighting -> CPU thermal die bug /0506
PROJECT : TW3
Quanta Computer Inc.
Size
Document Number
Yonah/Merom (Power/NC)
Rev 3A
Date: Thursday, June 15, 2006
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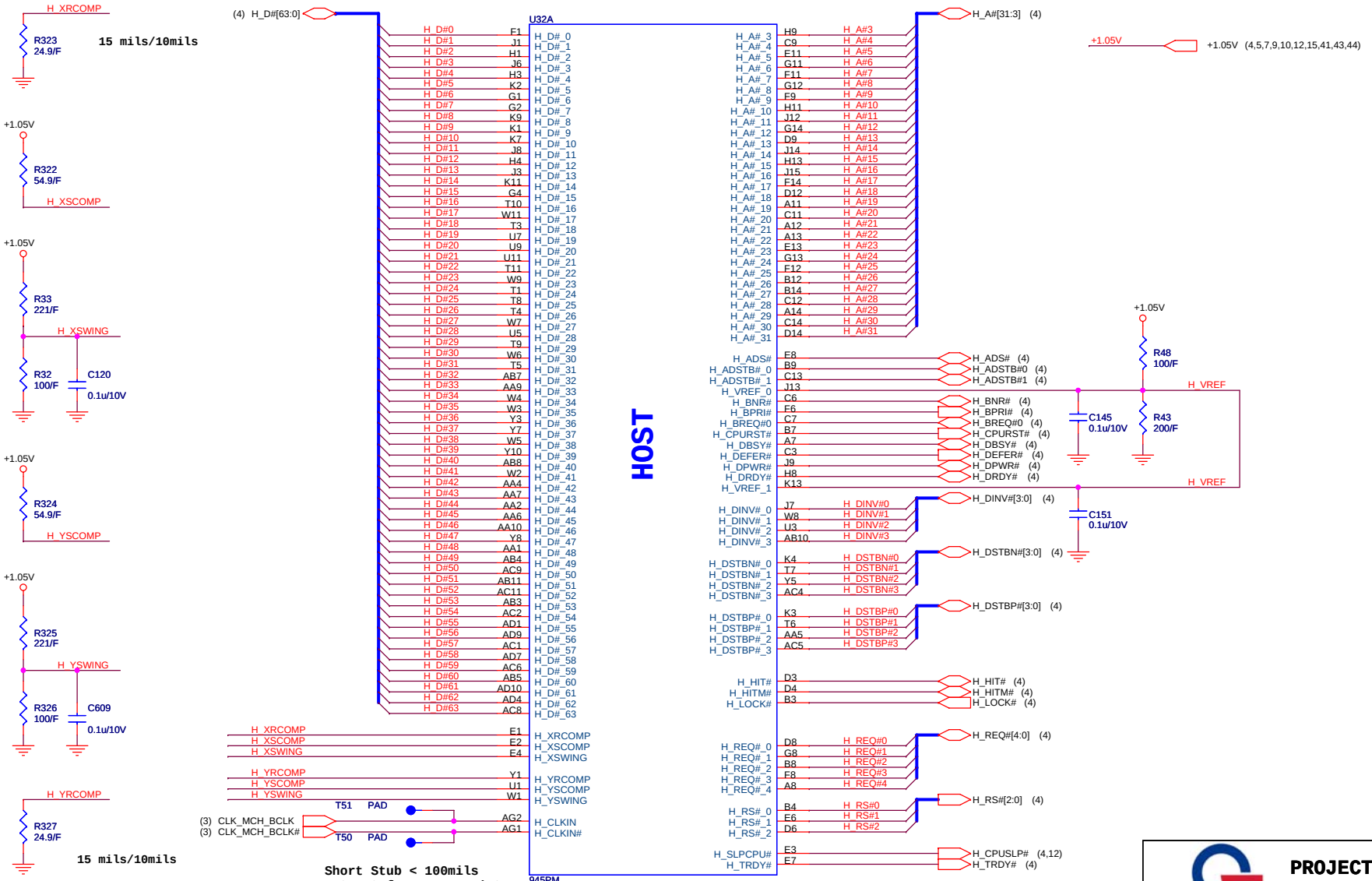
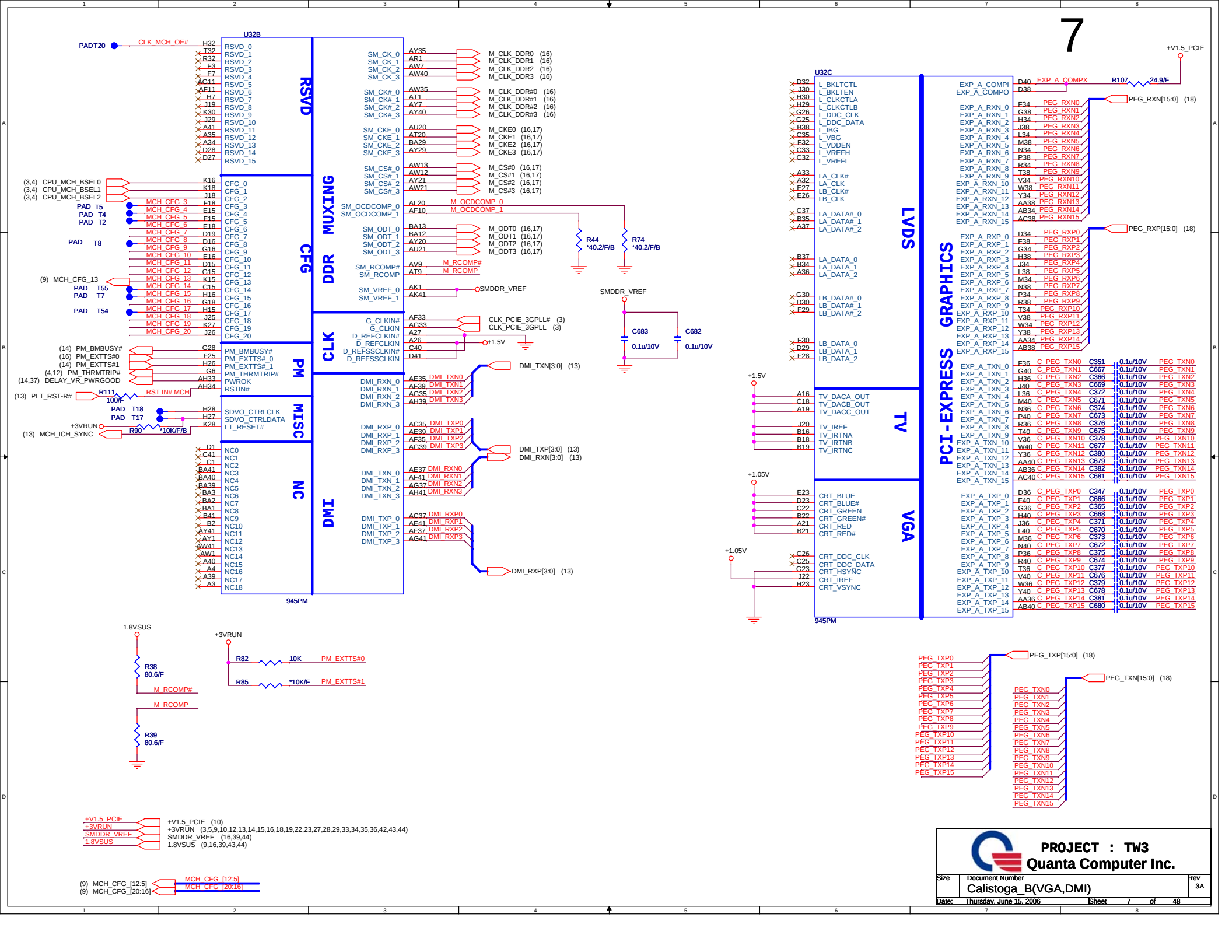
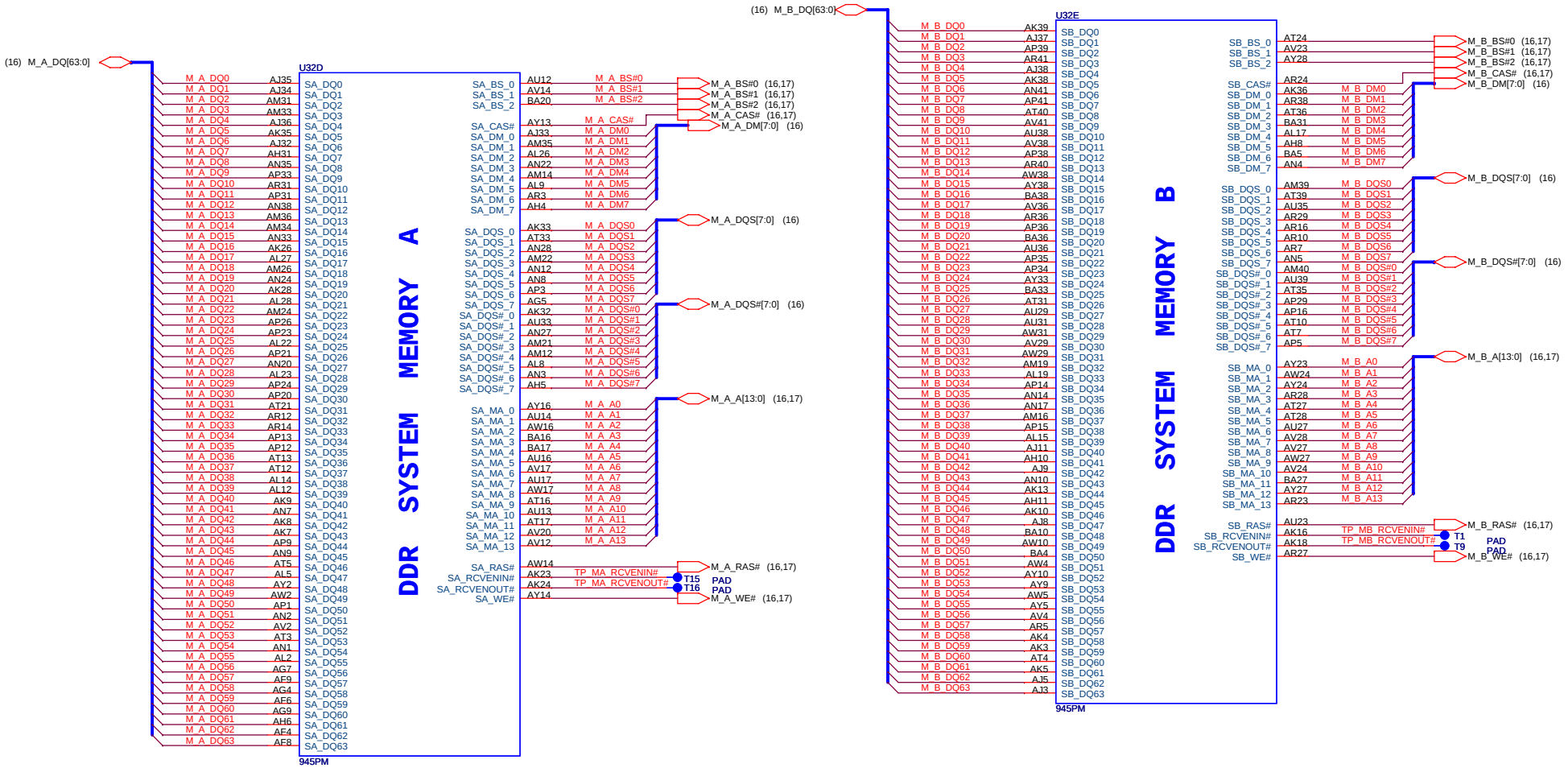


PROJECT : TW3
Quanta Computer Inc.

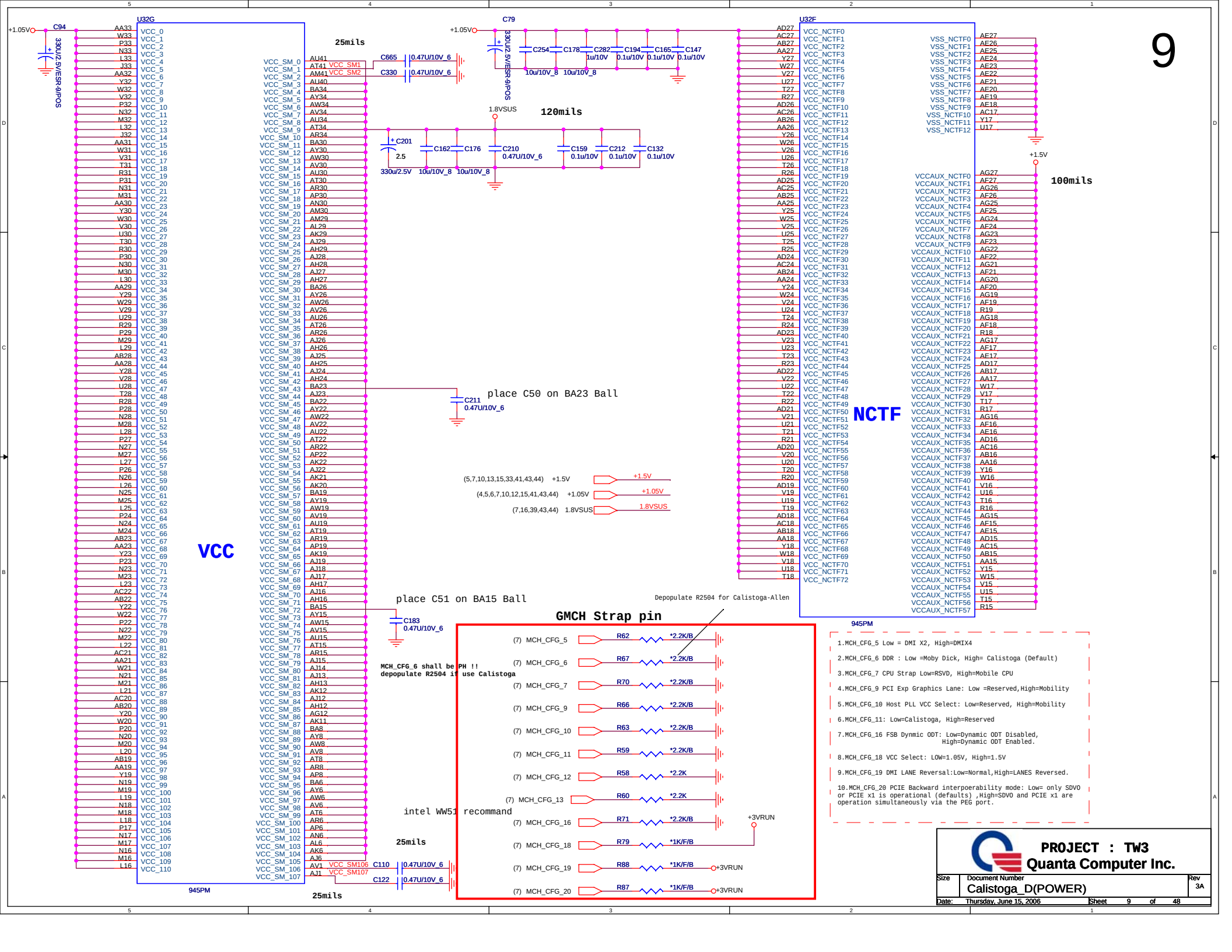
Size	Document Number	Rev
	Calistoga_A(Host)	3A

Date: Thursday, June 15, 2006 Sheet 6 of 48


U32B
RSVD
CFG
PM
MISC
NC
MUXING
DDR
CLK
DMI
945PM
U32C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
945PM
PROJECT : TW3
Quanta Computer Inc.
Calistoga_B(VGA,DMI)
Size
Document Number
Rev
3A
Date: Thursday, June 15, 2006
Sheet 7 of 48



PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number: Calistoga_C(DDR)	Rev: 3A
Date: Thursday, June 15, 2006	Sheet 8 of 48	


9
U32G
VCC
945PM
25mils
120mils
100mils
place C50 on BA23 Ball
place C51 on BA15 Ball
MCH_CFG_6 shall be PH !!
depopulate R2504 if use Calistoga
Depopulate R2504 for Calistoga-Allen
GMCH Strap pin
intel WW51 recommand
U32F
NCTF
945PM
1.MCH_CFG_5 Low = DMI X2, High=DMIX4
2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
6.MCH_CFG_11: Low=Calistoga, High=Reserved
7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.
PROJECT : TW3
Quanta Computer Inc.
Size
Document Number
Calistoga_D(POWER)
Rev 3A
Date: Thursday, June 15, 2006
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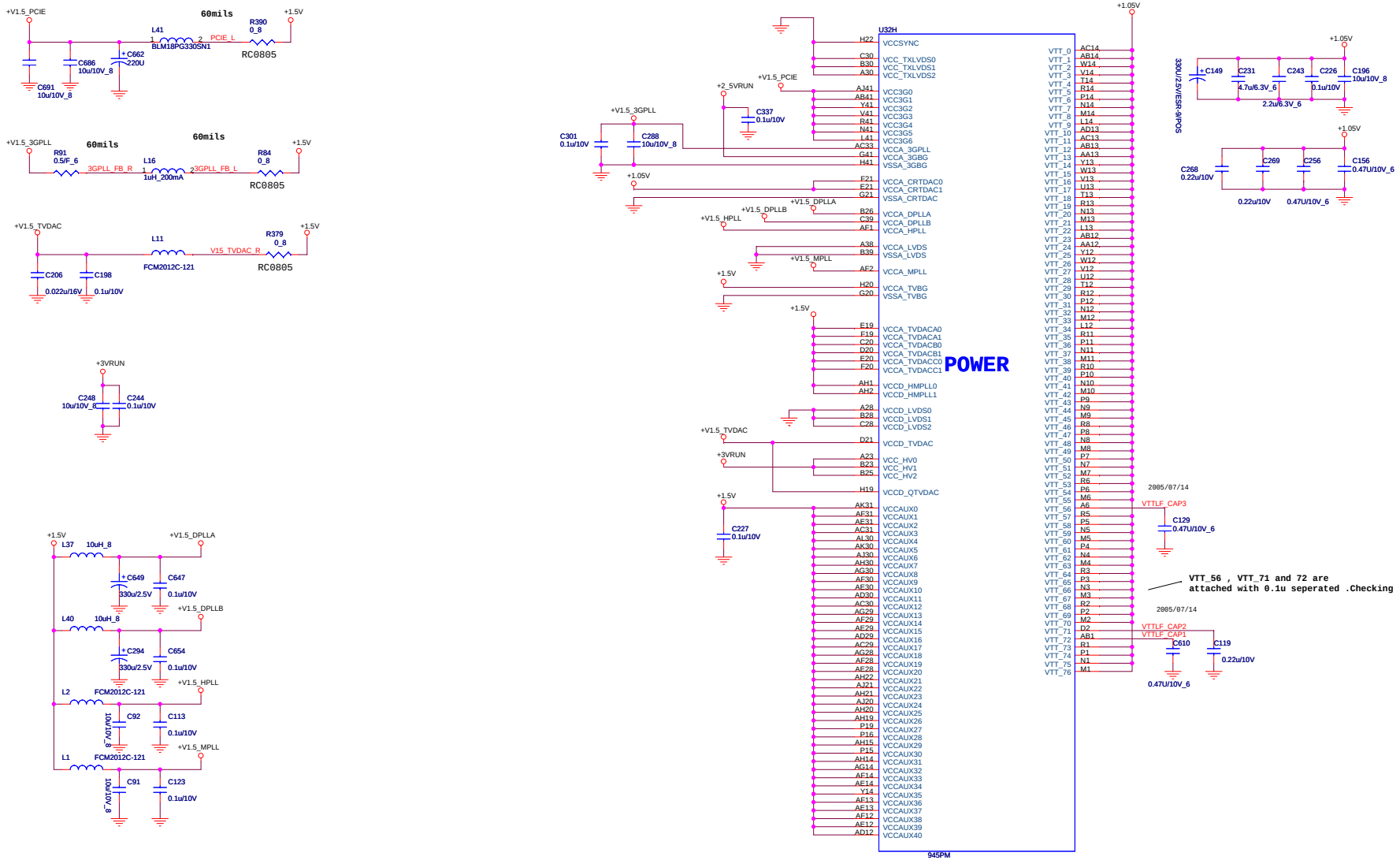
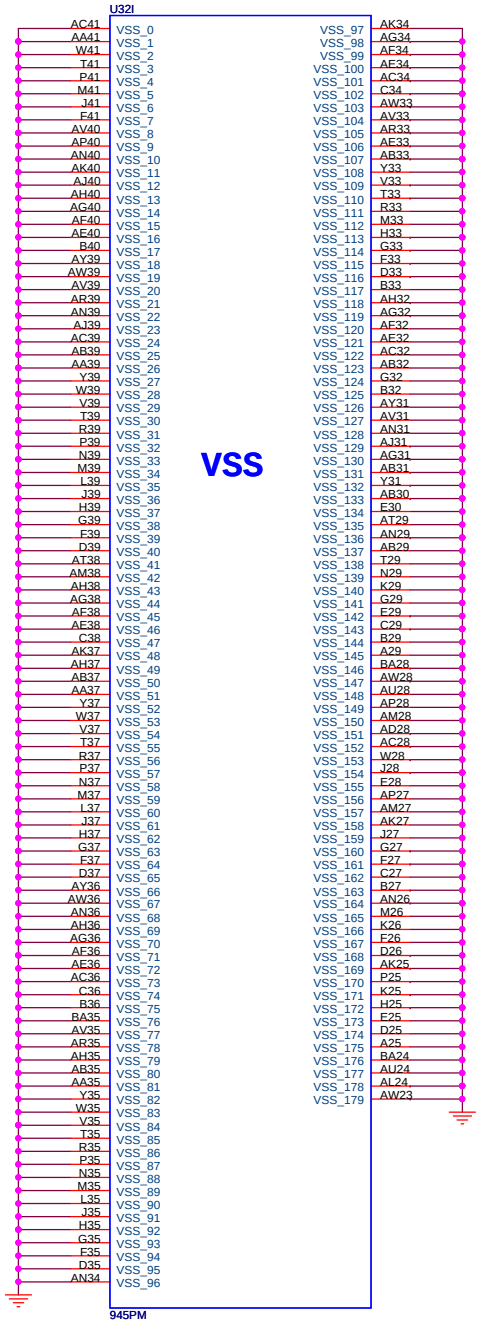
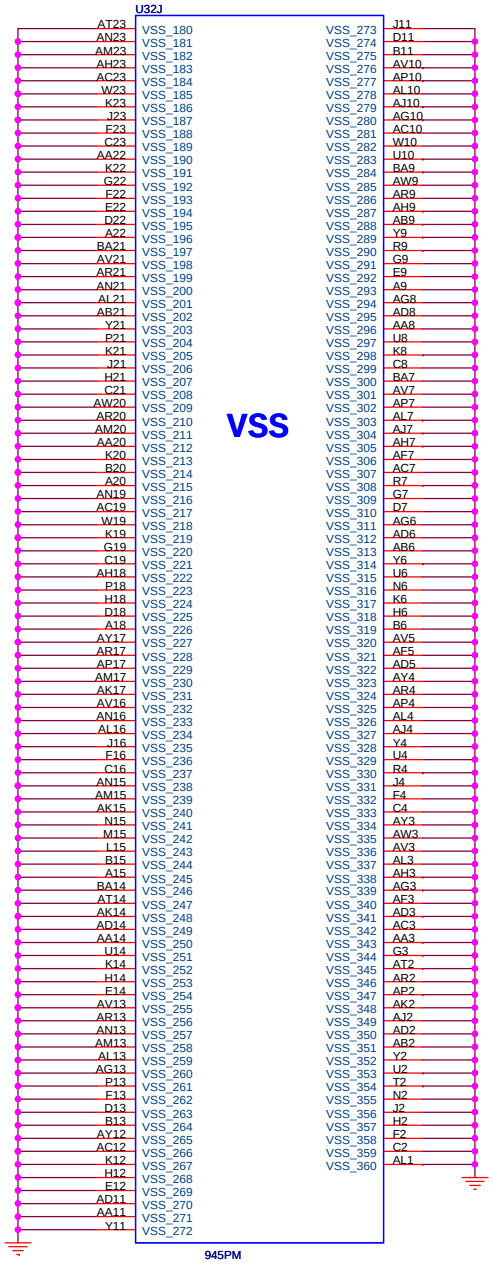


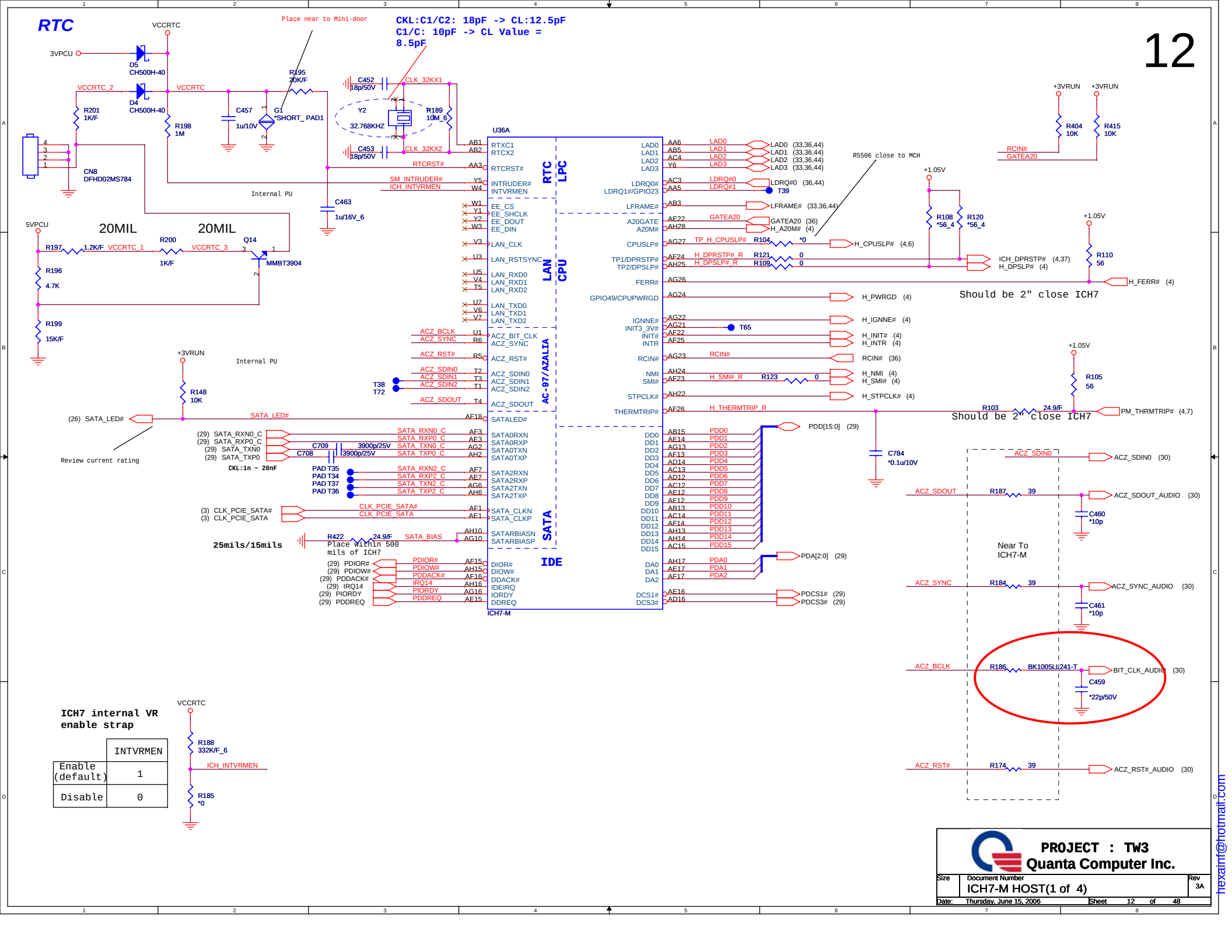
PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Calistoga_E(POWER2)	3A
Date: Thursday, June 15, 2006	Sheet 10 of 48	





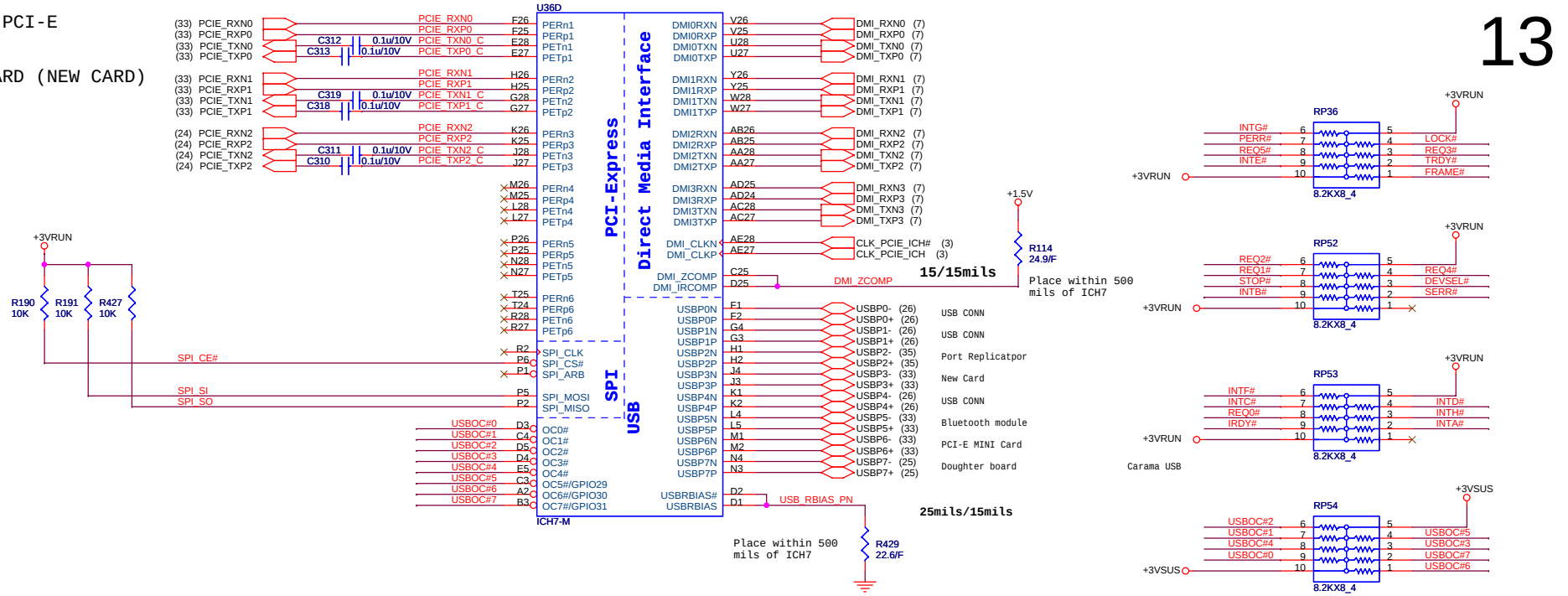
PROJECT : TW3			
Quanta Computer Inc.			
Size	Document Number		Rev
	Calistoga_F(VSS, NCTF)		3A
Date: Thursday, June 15, 2006	Sheet 11 of 48		

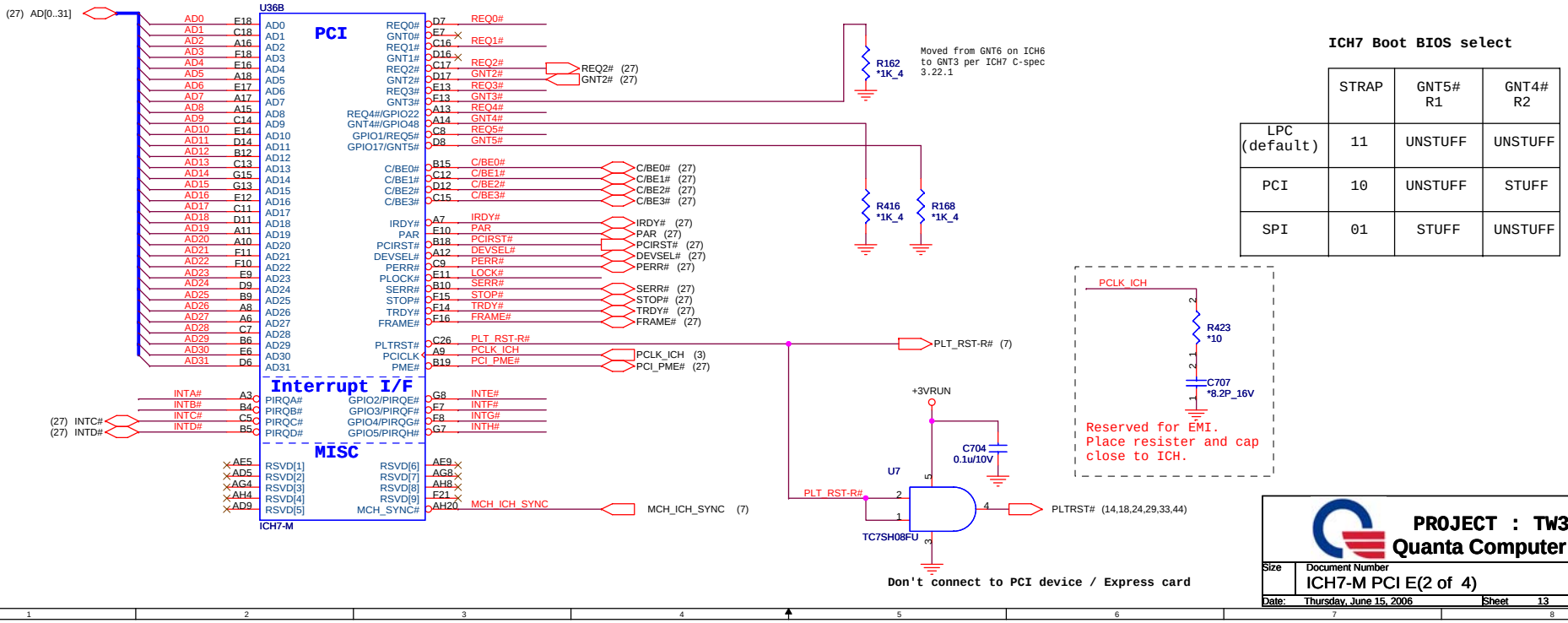

RTC
Place near to Mini-door
CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF
12
VCCRTC
3VPCU
D5 CH500H-40
VCCRTC_2
D4 CH500H-40
R195 20K/F
C452 18p/50V
CLK_32KX1
Y2 32.768KHZ
R189 10M_6
C453 18p/50V
CLK_32KX2
R201 1K/F
R198 1M
C457 1u/10V
G1 *SHORT_ PAD1
CN8 DFHD02MS784
Internal PU
C463 1u/16V_6
RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
U36A
RTXC1
RTXC2
RTCRST#
INTRUDER#
INTVRMEN
RTC
LPC
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN CPU
ACZ_BIT_CLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT
AC-97/AZALIA
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIASN
SATARBIASP
SATA
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
IDE
ICH7-M
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LDRQ1#/GPIO23
LFRAME#
A20GATE
A20M#
CPUSLP#
TP1/DPRSTP#
TP2/DPSLP#
FERR#
GPIO49/CPUPWRGD
IGNNE#
INIT3_3V#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THERMTRIP#
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
R5506 close to MCH
R104 *0
R121 0
R109 0
R123 0
T39
T65
T38
T72
+3VRUN
R404 10K
R415 10K
RCIN#
GATEA20
+1.05V
R108 *56_4
R120 *56_4
R110 56
R105 56
Should be 2" close ICH7
Should be 2" close ICH7
H_CPUSLP# (4,6)
ICH_DPRSTP# (4,37)
H_DPSLP# (4)
H_FERR# (4)
H_PWRGD (4)
H_IGNNE# (4)
H_INIT# (4)
H_INTR (4)
RCIN# (36)
H_NMI (4)
H_SMI# (4)
H_STPCLK# (4)
PM_THRMTRIP# (4,7)
PDD[15:0] (29)
PDA[2:0] (29)
PDCS1# (29)
PDCS3# (29)
C784 *0.1u/10V
5VPCU
20MIL
20MIL
R197 1.2K/F
R200 1K/F
Q14 MMBT3904
R196 4.7K
R199 15K/F
VCCRTC_1
VCCRTC_3
+3VRUN
R148 10K
Internal PU
(26) SATA_LED#
Review current rating
SATA_LED#
(29) SATA_RXN0_C
(29) SATA_RXP0_C
(29) SATA_TXN0
(29) SATA_TXP0
C709 3900p/25V
C708 3900p/25V
CKL:in ~ 20nF
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
PAD T35
PAD T34
PAD T37
PAD T36
SATA_RXN2_C
SATA_RXP2_C
SATA_TXN2_C
SATA_TXP2_C
(3) CLK_PCIE_SATA#
(3) CLK_PCIE_SATA
CLK_PCIE_SATA#
CLK_PCIE_SATA
R422 24.9/F
SATA_BIAS
Place within 500 mils of ICH7
25mils/15mils
(29) PDIOR#
(29) PDIOW#
(29) PDDACK#
(29) IRQ14
(29) PIORDY
(29) PDDREQ
PDIOR#
PDIOW#
PDDACK#
IRQ14
PIORDY
PDDREQ
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDOUT
R187 39
R184 39
R186 BK1005LI241-T
R174 39
ACZ_SDOUT_AUDIO (30)
ACZ_SYNC_AUDIO (30)
BIT_CLK_AUDIO (30)
ACZ_RST#_AUDIO (30)
C460 *10p
C461 *10p
C459 *22p/50V
Near To ICH7-M
ICH7 internal VR enable strap
INTVRMEN
Enable (default) 1
Disable 0
R188 332K/F_6
R185 *0
PROJECT : TW3
Quanta Computer Inc.
Size
Document Number
ICH7-M HOST(1 of 4)
Rev 3A
Date: Thursday, June 15, 2006
Sheet 12 of 48
hexainf@hotmail.com

MINI CARD PCI-E

EXPRESS CARD (NEW CARD)

13





ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M PCI E(2 of 4)	3A

Date: Thursday, June 15, 2006 Sheet 13 of 48

R376

No stuff-->boot
Stuff-->No boot

+3V_S5
PCLK_SMB R124 2.2K
PDAT_SMB R128 2.2K
PCIE_WAKE# R156 680

+3V_S5
RI# R389 10K
SMB_LINK_ALERT# R391 10K
SMLINK0 R392 10K
SMLINK1 R394 10K
EXTSMI#_R R153 *10K
WAKE_SCI#_R R95 10K
SMBALERT# R395 10K

+3V_S5
SWI# R409 10K
DNBSWON# R117 10K
SYS_RST# R396 10K
PM_BATLOW# R401 8.2K/F

+3VRUN
SYS_RST# R399 *10K
CLKRUN# R420 8.2K/F
SERIRQ R412 8.2K/F
RUNTIME_SCI#_R R140 10K

RSMRST# R424 10K

SYS_RST is suspend rail

U36C

+3VRUN
R411 *1K_4
(30) ACZ_SPKR

(3,33) PCLK_SMB
(3,33) PDAT_SMB
PCLK_SMB C22
PDAT_SMB B22
SMB_LINK_ALERT# A26
SMLINK0 B25
SMLINK1 A25
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
SMB

(27) RI#
RI# A28
RI#

A19
SPKR
(27,44) SUS_STAT#
(4) SYS_RST#
SUS_STAT# A27
SYS_RST# A22
SUS_STAT#
SYS_RST#

(7) PM_BMBUSY#
R166 0
AB18
GPIO0/BM_BUSY#

T24
SMBALERT# B23
GPIO11/SMBALERT#

No ASF support
(3) PM_STPPCI#
(3) PM_STPCPU#
R130 0
R127 0
PM_STPPCI_ICH# AC20
PM_STPCPU_ICH# AF21
GPIO18/STPPCI#
GPIO20/STPCPU#

T64
A21
GPIO26

T66
T22
B21
F23
GPIO27
GPIO28

(27,36,44) CLKRUN#
CLKRUN# AG18
GPIO32/CLKRUN#

(29) ICH_GPO33
ICH_GPO33 AC19
BOARD_ID2 U2
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#

(24,33) PCIE_WAKE#
(27,36,44) SERIRQ
PCIE_WAKE# F20
SERIRQ AH21
THRM# AF20
WAKE#
SERIRQ
THRM#

(5) THERM_ALERT#

VR_PWRGD_CK410 AD22
VRMPWRGD

T28
(36) SCI#
(36) KBSMI#
R141 0
R143 0
RUNTIME_SCI#_R AC21
EXTSMI#_R AC18
F21
GPIO6
GPIO7
GPIO8

ICH7-M

SYS GPIO

Power MGT

GPIO

SATA GPIO

Clocks

GPIO21/SATA0GP AE19 BOARD_ID1
GPIO19/SATA1GP AH18 BOARD_ID0
GPIO36/SATA2GP AH19 BOARD_ID3
GPIO37/SATA3GP AE19 BOARD_ID4

CLK14 AC1 14M_ICH
CLK48 B2 CLKUSB_48
14M_ICH (3)
CLKUSB_48 (3)

SUSCLK C20 ICH_SUSCLK
T31

SLP_S3# B24 R115 100/F
SLP_S4# D23 R122 100/F
SLP_S5# F22
SUSB# (36)
SUSC# (36)
T21

PWROK AA4 ICH_PWROK

GPIO16/DPRSLPVR AC22 PM_DPRSLPVR_R R113 100/F
PM_EXTTS#1 (7)
PM_DPRSLPVR (37)
R116 0
R112 *100K

TP0/BATLOW# C21 PM_BATLOW#_R R400 100/F
PM_BATLOW# (36)

PWRBTN# C23 DNBSWON#
R158 100K
DNBSWON# (36)

LAN_RST# C19
R98 0
PLTRST# (13,18,24,29,33,44)

RSMRST# Y4 PM_RSMRST#_R R425 100/F RSMRST#
RSMRST# (36)

GPIO9 F20 SWI#
GPIO10 A20 T67
GPIO12 E19 T27
GPIO13 R4 WAKE_SCI#_R T19
GPIO14 F22 T40
GPIO15 R3 T25
GPIO24 D20 T29
GPIO25 AD21
GPIO35 AD20 GPIO38
GPIO38 AE20 T30
GPIO39

SWI# (36)

CKL :100Kohm PD

+3VRUN
U14
(3,37) CLK_EN#
VR_PWRGD_CK410
NL17SZ14DFT2G

Note: External pull-up 3V

GPIO25 /Suspend rail is a HW strap , don't pull down .

PWM require 6.9K
Change to 6.8K
+3VSUS
C451 0.047u/10V
+3VRUN
R193 6.8K
U15
(7,37) DELAY_VR_PWRGOOD
(36) PWROK
R182 100K
TC7SH08FU
ICH_PWROK
R183 10K

Level is incorrect !!

Place these close to ICH7.
CLKUSB_48
R428 *10
C712 *4.7P_50V
14M_ICH
R372 *10_NC
C637 *4.7P_50V_NC

+3VRUN
R421 *10K_4
BOARD_ID0
R167 10K

+3VRUN
R147 *10K
BOARD_ID1
R139 10K

+3VRUN
R371 *10K_NC
BOARD_ID2
R367 10K

+3VRUN
R136 *10K
BOARD_ID3
R137 10K

+3VRUN
R368 10K
BOARD_ID4
R366 *10K

+3VRUN
R482 10K
GPIO38
R483 *10K

GPIO38	Function
High	CRT
Low	DVI

Board ID	Function
ID [1:0]	00: TW3 01: DW1
ID2	0: SATA HDD 1: PATA HDD
ID3	Reserve
ID4	0: No docking. 1: w/ docking

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M GPIO(3 of 4)	3B

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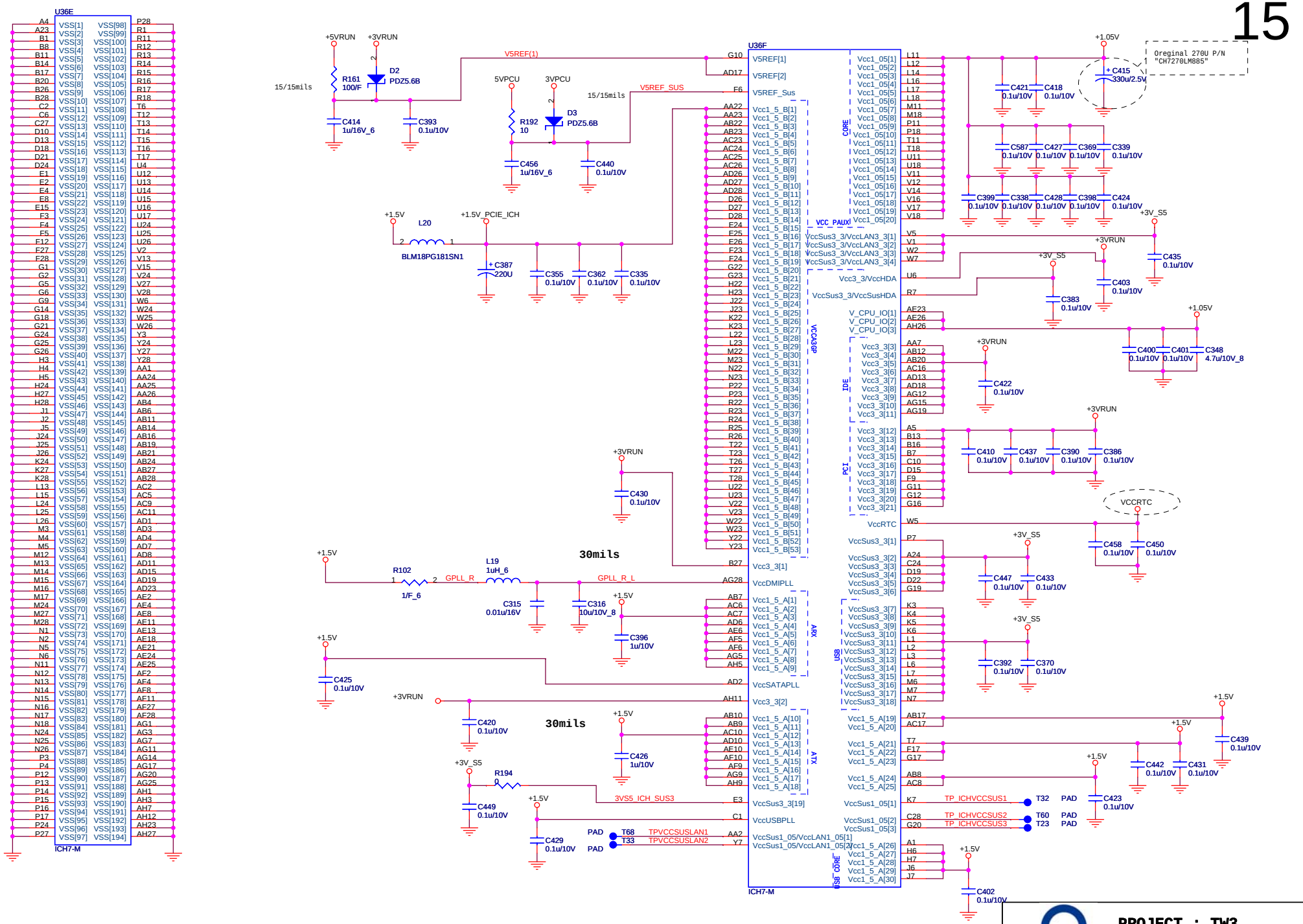

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M POWER(4 of 4)	3A

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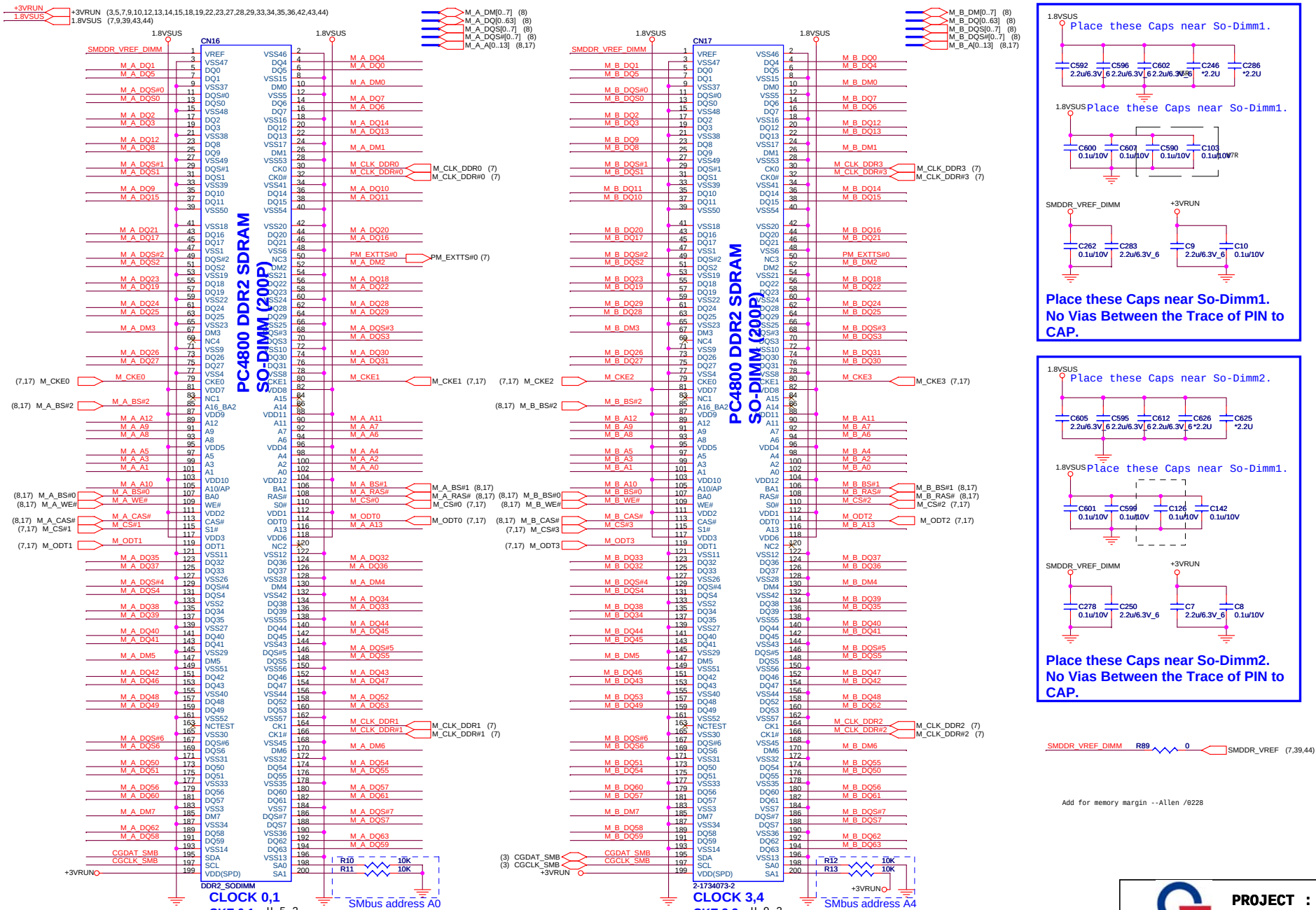

1.8VSUS

Place these Caps near So-Dimm1.

C592 2.2u/6.3V_6 C596 2.2u/6.3V_6 C602 2.2u/6.3V_6 C246 *2.2U C286 *2.2U

1.8VSUS Place these Caps near So-Dimm1.

C600 0.1u/10V C607 0.1u/10V C590 0.1u/10V C103 0.1u/10V

SMDDR_VREF_DIMM

C262 0.1u/10V C283 2.2u/6.3V_6

+3VRUN

C9 2.2u/6.3V_6 C10 0.1u/10V

Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

1.8VSUS

Place these Caps near So-Dimm2.

C605 2.2u/6.3V_6 C595 2.2u/6.3V_6 C612 2.2u/6.3V_6 C626 *2.2U C625 *2.2U

1.8VSUS Place these Caps near So-Dimm1.

C601 0.1u/10V C599 0.1u/10V C126 0.1u/10V C142 0.1u/10V

SMDDR_VREF_DIMM

C278 0.1u/10V C250 2.2u/6.3V_6

+3VRUN

C7 2.2u/6.3V_6 C8 0.1u/10V

Place these Caps near So-Dimm2.
No Vias Between the Trace of PIN to CAP.

SMDDR_VREF_DIMM R89 0 SMDDR_VREF (7,39,44)

Add for memory margin --Allen /0228

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	DDRII SO-DIMM(200P)	3A

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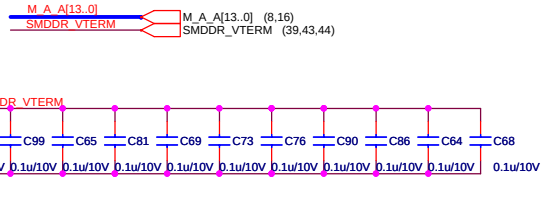
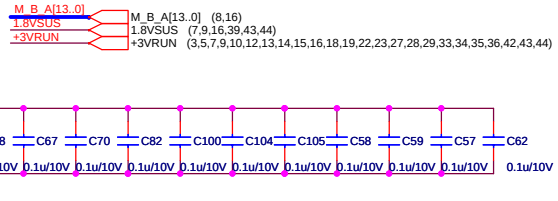
DDRII DUAL CHANNEL A,B.

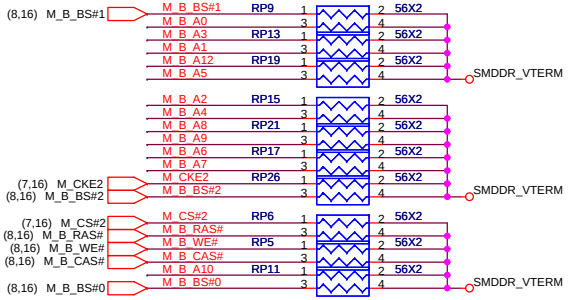
DDRII A CHANNEL

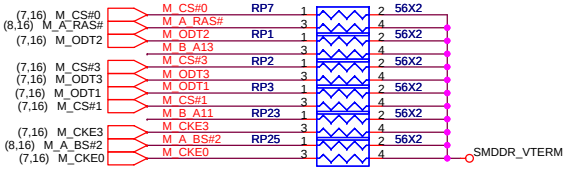


DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM





PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number: DDRII TERMINATION	Rev: 3A
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(7) PEG_RXP[15:0]
(7) PEG_RXN[15:0]
(7) PEG_TXP[15:0]
(7) PEG_TXN[15:0]

U31A
PART 1 OF 4
PCI-EXPRESS INTERFACE
Clock
PCIE Power
G72M

PEG_TXP0 AF1 PEX_RX0P
PEG_TXN0 AG2 PEX_RX0N
PEG_TXP1 AG3 PEX_RX1P
PEG_TXN1 AG4 PEX_RX1N
PEG_TXP2 AE4 PEX_RX2P
PEG_TXN2 AF5 PEX_RX2N
PEG_TXP3 AG6 PEX_RX3P
PEG_TXN3 AG7 PEX_RX3N
PEG_TXP4 AF7 PEX_RX4P
PEG_TXN4 AF8 PEX_RX4N
PEG_TXP5 AG9 PEX_RX5P
PEG_TXN5 AG10 PEX_RX5N
PEG_TXP6 AE10 PEX_RX6P
PEG_TXN6 AF11 PEX_RX6N
PEG_TXP7 AG12 PEX_RX7P
PEG_TXN7 AG13 PEX_RX7N
PEG_TXP8 AG15 PEX_RX8P
PEG_TXN8 AG16 PEX_RX8N
PEG_TXP9 AF16 PEX_RX9P
PEG_TXN9 AF17 PEX_RX9N
PEG_TXP10 AG18 PEX_RX10P
PEG_TXN10 AG19 PEX_RX10N
PEG_TXP11 AF19 PEX_RX11P
PEG_TXN11 AF20 PEX_RX11N
PEG_TXP12 AG21 PEX_RX12P
PEG_TXN12 AG22 PEX_RX12N
PEG_TXP13 AF22 PEX_RX13P
PEG_TXN13 AF23 PEX_RX13N
PEG_TXP14 AG24 PEX_RX14P
PEG_TXN14 AG25 PEX_RX14N
PEG_TXP15 AG26 PEX_RX15P
PEG_TXN15 AF27 PEX_RX15N

(3) CLK_PCIE_VGA AE3 PEX_REFCLK
(3) CLK_PCIE_VGA# AE4 PEX_REFCLK#

PEX_TX0P AD5 V_GMCHEXP_RXP0
PEX_TX0N AD6 V_GMCHEXP_RXN0
PEX_TX1P AE6 V_GMCHEXP_RXP1
PEX_TX1N AE7 V_GMCHEXP_RXN1
PEX_TX2P AD7 V_GMCHEXP_RXP2
PEX_TX2N AC7 V_GMCHEXP_RXN2
PEX_TX3P AE9 V_GMCHEXP_RXP3
PEX_TX3N AE10 V_GMCHEXP_RXN3
PEX_TX4P AD10 V_GMCHEXP_RXP4
PEX_TX4N AC10 V_GMCHEXP_RXN4
PEX_TX5P AE12 V_GMCHEXP_RXP5
PEX_TX5N AE13 V_GMCHEXP_RXN5
PEX_TX6P AD13 V_GMCHEXP_RXP6
PEX_TX6N AC13 V_GMCHEXP_RXN6
PEX_TX7P AC15 V_GMCHEXP_RXP7
PEX_TX7N AD15 V_GMCHEXP_RXN7
PEX_TX8P AE15 V_GMCHEXP_RXP8
PEX_TX8N AE16 V_GMCHEXP_RXN8
PEX_TX9P AC18 V_GMCHEXP_RXP9
PEX_TX9N AD18 V_GMCHEXP_RXN9
PEX_TX10P AE18 V_GMCHEXP_RXP10
PEX_TX10N AE19 V_GMCHEXP_RXN10
PEX_TX11P AC21 V_GMCHEXP_RXP11
PEX_TX11N AD21 V_GMCHEXP_RXN11
PEX_TX12P AE21 V_GMCHEXP_RXP12
PEX_TX12N AE22 V_GMCHEXP_RXN12
PEX_TX13P AD22 V_GMCHEXP_RXP13
PEX_TX13N AD23 V_GMCHEXP_RXN13
PEX_TX14P AE25 V_GMCHEXP_RXP14
PEX_TX14N AE25 V_GMCHEXP_RXN14
PEX_TX15P AE24 V_GMCHEXP_RXP15
PEX_TX15N AD24 V_GMCHEXP_RXN15

PEX_TSTCLK_OUT AF13 PEX_TSTCLK
PEX_TSTCLK_OUT# AF14 PEX_TSTCLK#
PEX_RST# AC6

R93 *200/F
R386 0

U33 *TC7SH08FU
PLTRST# (13,14,24,29,33,44)

PEX_IOVDD_01 AB10
PEX_IOVDD_02 AB11
PEX_IOVDD_03 AB14
PEX_IOVDD_04 AB15
PEX_IOVDD_05 W17
PEX_IOVDD_06 W18
PEX_IOVDD_07 AB20
PEX_IOVDD_08 AB21

PEX_IOVDDQ_01 AA4
PEX_IOVDDQ_02 AB5
PEX_IOVDDQ_03 AB6
PEX_IOVDDQ_04 AB7
PEX_IOVDDQ_05 AB8
PEX_IOVDDQ_06 AB9
PEX_IOVDDQ_07 AC9
PEX_IOVDDQ_08 AC11
PEX_IOVDDQ_09 AB12
PEX_IOVDDQ_10 AC12
PEX_IOVDDQ_11 AB13
PEX_IOVDDQ_12 AB16
PEX_IOVDDQ_13 AC16
PEX_IOVDDQ_14 AB17
PEX_IOVDDQ_15 AC17
PEX_IOVDDQ_16 AB18
PEX_IOVDDQ_17 AB19
PEX_IOVDDQ_18 AC19
PEX_IOVDDQ_19 AC20

VDD_LP_01 W9
VDD_LP_02 W10
VDD_LP_03 W11
VDD_LP_04 W12

VDD33_01 J12
VDD33_02 F13
VDD33_03 J13
VDD33_04 F14
VDD33_05 J15
VDD33_06 J16

NC_01 D12
NC_02 E12
NC_03 F12
NC_04 C13

PEX_PLLVDD Y6
PEX_PLLDVDD AA5
PEX_PLLGND AA6

VDD_01 J9
VDD_02 M9
VDD_03 N9
VDD_04 R9
VDD_05 T9
VDD_06 J10
VDD_07 J11
VDD_08 M11
VDD_09 N11
VDD_10 R11
VDD_11 T11
VDD_12 L12
VDD_13 M12
VDD_14 T12
VDD_15 U12
VDD_16 L13
VDD_17 M13
VDD_18 T13
VDD_19 U13
VDD_20 W13
VDD_21 M14
VDD_22 T14
VDD_23 L15
VDD_24 M15
VDD_25 T15
VDD_26 U15
VDD_27 W15
VDD_28 L16
VDD_29 M16
VDD_30 T16
VDD_31 U16
VDD_32 W16
VDD_33 M17
VDD_34 N17
VDD_35 R17
VDD_36 T17

G72_PLLAVDD

PEG_RXP0 C304 V_GMCHEXP_RXP0
PEG_RXP1 C314 V_GMCHEXP_RXP1
PEG_RXP2 C664 V_GMCHEXP_RXP2
PEG_RXP3 C326 V_GMCHEXP_RXP3
PEG_RXP4 C684 V_GMCHEXP_RXP4
PEG_RXP5 C368 V_GMCHEXP_RXP5
PEG_RXP6 C688 V_GMCHEXP_RXP6
PEG_RXP7 C385 V_GMCHEXP_RXP7
PEG_RXP8 C690 V_GMCHEXP_RXP8
PEG_RXP9 C353 V_GMCHEXP_RXP9
PEG_RXP10 C693 V_GMCHEXP_RXP10
PEG_RXP11 C361 V_GMCHEXP_RXP11
PEG_RXP12 C696 V_GMCHEXP_RXP12
PEG_RXP13 C364 V_GMCHEXP_RXP13
PEG_RXP14 C699 V_GMCHEXP_RXP14
PEG_RXP15 V_GMCHEXP_RXP15

PEG_RXN0 C309 V_GMCHEXP_RXN0
PEG_RXN1 C657 V_GMCHEXP_RXN1
PEG_RXN2 C323 V_GMCHEXP_RXN2
PEG_RXN3 C663 V_GMCHEXP_RXN3
PEG_RXN4 C332 V_GMCHEXP_RXN4
PEG_RXN5 C685 V_GMCHEXP_RXN5
PEG_RXN6 C367 V_GMCHEXP_RXN6
PEG_RXN7 C687 V_GMCHEXP_RXN7
PEG_RXN8 C384 V_GMCHEXP_RXN8
PEG_RXN9 C689 V_GMCHEXP_RXN9
PEG_RXN10 C352 V_GMCHEXP_RXN10
PEG_RXN11 C692 V_GMCHEXP_RXN11
PEG_RXN12 C360 V_GMCHEXP_RXN12
PEG_RXN13 C695 V_GMCHEXP_RXN13
PEG_RXN14 C363 V_GMCHEXP_RXN14
PEG_RXN15 C698 V_GMCHEXP_RXN15

+1.2V_GFX_PCIE
L14 BLM11A121S
C242 4.7u/6.3V_6
C192 0.1u/10V

+3VRUN
C651 *0.1u/10V

+VCC_GFX_CORE
C247 100p/50V
C189 0.01u/16V
C197 0.01u/16V
C168 100p/50V
C181 0.01u/16V
C228 220p/50V
C240 100p/50V
C223 220p/50V
C205 100p/50V
C170 1u/10V
C224 220p/50V
C185 0.01u/16V
C238 220p/50V
C225 220p/50V
C219 10u/6.3V_6
C245 10u/6.3V_6
C188 10u/6.3V_6

+1.2V_GFX_PCIE
C266 0.022u/16V
C274 0.022u/16V
C273 0.022u/16V
C258 10u/6.3V_6
C261 1u/10V
C277 4.7u/6.3V_6
PLACE NEAR BALLS
PLACE NEAR GPU

+1.2V_GFX_PCIE
C259 10u/6.3V_6
C271 0.022u/16V
C276 0.1u/10V
C272 0.1u/10V
C260 1u/10V
C606 4.7u/6.3V_6
PLACE NEAR BALLS

+VCC_GFX_CORE
C209 220p/50V
C193 0.01u/16V
C249 0.1u/10V

+1.2V_GFX_PCIE
L17 BLM11A121S
C285 4.7u/6.3V_6
C281 1u/10V
C280 1u/10V
C241 0.1u/10V
C255 0.01u/16V

+3VRUN
C169 0.1u/10V
C173 4700p/25V
C230 0.022u/16V
C155 1u/10V
PLACE NEAR BALLS

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	NV72M-1	3A

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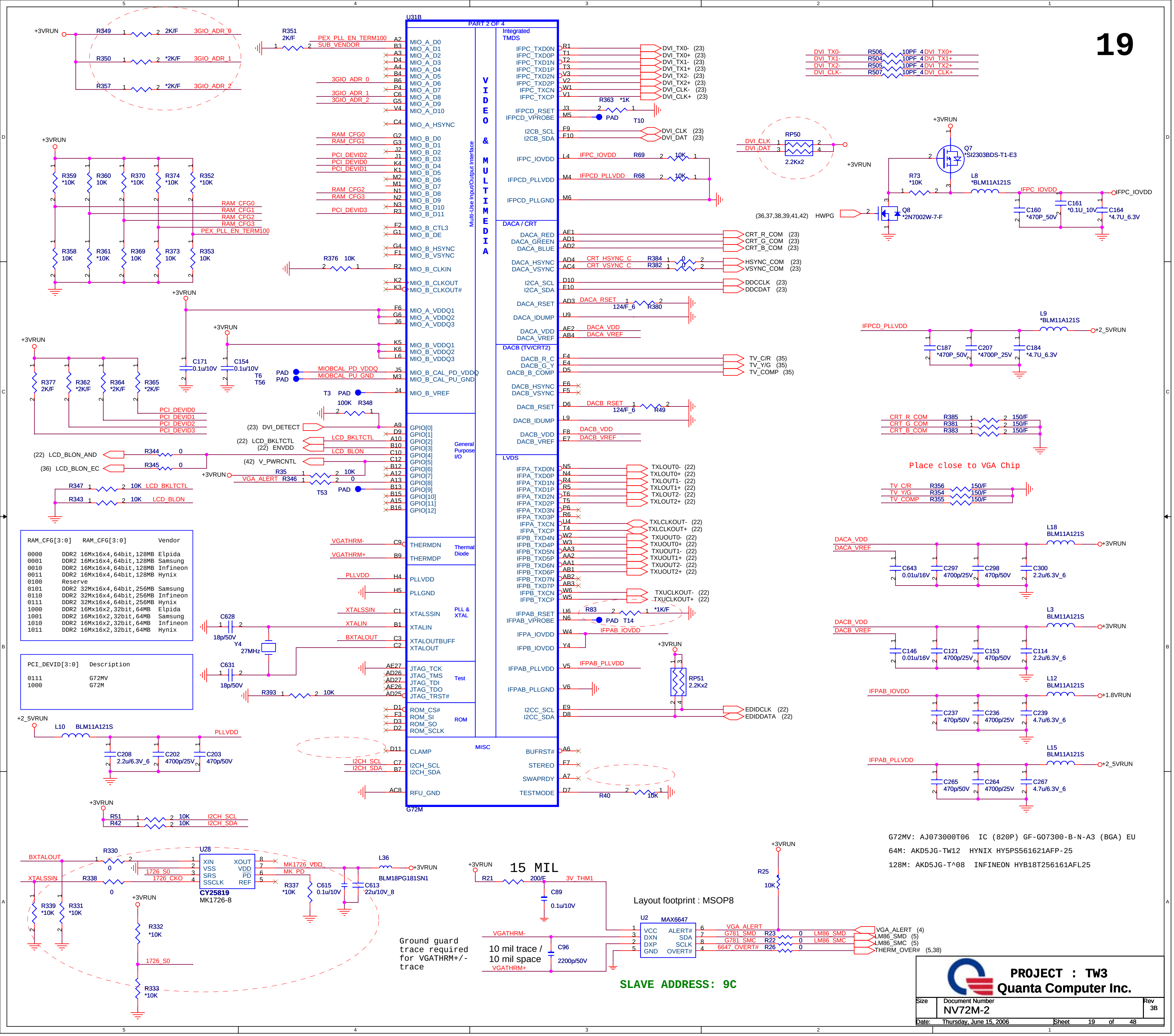


RAM_CFG[3:0]	RAM_CFG[3:0]	Vendor
0000	DDR2 16Mx16x4,64bit,128MB	Elpida
0001	DDR2 16Mx16x4,64bit,128MB	Samsung
0010	DDR2 16Mx16x4,64bit,128MB	Infineon
0011	DDR2 16Mx16x4,64bit,128MB	Hynix
0100	Reserve	
0101	DDR2 32Mx16x4,64bit,256MB	Samsung
0110	DDR2 32Mx16x4,64bit,256MB	Infineon
0111	DDR2 32Mx16x4,64bit,256MB	Hynix
1000	DDR2 16Mx16x2,32bit,64MB	Elpida
1001	DDR2 16Mx16x2,32bit,64MB	Samsung
1010	DDR2 16Mx16x2,32bit,64MB	Infineon
1011	DDR2 16Mx16x2,32bit,64MB	Hynix

PCI_DEVID[3:0]	Description
0111	G72MV
1000	G72M

G72MV: AJ073000T06 IC (820P) GF-GO7300-B-N-A3 (BGA) EU

64M: AKD5JG-TW12 HYNIX HY5PS561621AFP-25

128M: AKD5JG-T^08 INFINEON HYB18T256161AFL25

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	NV72M-2	3B

Date: Thursday, June 15, 2006 Sheet 19 of 48

FB_CMD[0..26] (21)
FBD[0..63] (21)
FBDQM[0..7] (21)
FBDQS[0..7] (21)
FBDQS#[0..7] (21)

U31C

Part 3 of 4

MEMORY INTERFACE

FBD0	A26	FB_DQ0	
FBD1	C24	FB_DQ1	
FBD2	B24	FB_DQ2	
FBD3	A24	FB_DQ3	
FBD4	C22	FB_DQ4	
FBD5	A25	FB_DQ5	
FBD6	B25	FB_DQ6	
FBD7	D23	FB_DQ7	
FBD8	G22	FB_DQ8	
FBD9	J23	FB_DQ9	
FBD10	E24	FB_DQ10	
FBD11	F23	FB_DQ11	
FBD12	J24	FB_DQ12	
FBD13	F24	FB_DQ13	
FBD14	G23	FB_DQ14	
FBD15	H24	FB_DQ15	
FBD16	D16	FB_DQ16	
FBD17	E16	FB_DQ17	
FBD18	D17	FB_DQ18	
FBD19	E18	FB_DQ19	
FBD20	E19	FB_DQ20	
FBD21	E18	FB_DQ21	
FBD22	D20	FB_DQ22	
FBD23	D19	FB_DQ23	
FBD24	A18	FB_DQ24	
FBD25	B18	FB_DQ25	
FBD26	A19	FB_DQ26	
FBD27	B19	FB_DQ27	
FBD28	D18	FB_DQ28	
FBD29	C19	FB_DQ29	
FBD30	C16	FB_DQ30	
FBD31	C18	FB_DQ31	
FBD32	N26	FB_DQ32	
FBD33	N25	FB_DQ33	
FBD34	R25	FB_DQ34	
FBD35	R26	FB_DQ35	
FBD36	R27	FB_DQ36	
FBD37	T25	FB_DQ37	
FBD38	T27	FB_DQ38	
FBD39	T26	FB_DQ39	
FBD40	AB23	FB_DQ40	
FBD41	Y24	FB_DQ41	
FBD42	AB24	FB_DQ42	
FBD43	AB22	FB_DQ43	
FBD44	AC24	FB_DQ44	
FBD45	AC22	FB_DQ45	
FBD46	AA23	FB_DQ46	
FBD47	AA22	FB_DQ47	
FBD48	T24	FB_DQ48	
FBD49	T23	FB_DQ49	
FBD50	R24	FB_DQ50	
FBD51	R23	FB_DQ51	
FBD52	R22	FB_DQ52	
FBD53	T22	FB_DQ53	
FBD54	N23	FB_DQ54	
FBD55	P24	FB_DQ55	
FBD56	AA24	FB_DQ56	
FBD57	AA27	FB_DQ57	
FBD58	AA26	FB_DQ58	
FBD59	AB25	FB_DQ59	
FBD60	AB26	FB_DQ60	
FBD61	AB27	FB_DQ61	
FBD62	AA25	FB_DQ62	
FBD63	W25	FB_DQ63	

FB_CMD0	G27	FB_CMD0	
FB_CMD1	D25	FB_CMD1	
FB_CMD2	F26	FB_CMD2	
FB_CMD3	F25	FB_CMD3	
FB_CMD4	G25	FB_CMD4	
FB_CMD5	J25	FB_CMD5	
FB_CMD6	J27	FB_CMD6	
FB_CMD7	M26	FB_CMD7	
FB_CMD8	C27	FB_CMD8	
FB_CMD9	C25	FB_CMD9	
FB_CMD10	D24	FB_CMD10	
FB_CMD11	N27	FB_CMD11	
FB_CMD12	G24	FB_CMD12	
FB_CMD13	J26	FB_CMD13	
FB_CMD14	M27	FB_CMD14	
FB_CMD15	C26	FB_CMD15	
FB_CMD16	M25	FB_CMD16	
FB_CMD17	D26	FB_CMD17	
FB_CMD18	D27	FB_CMD18	
FB_CMD19	K26	FB_CMD19	
FB_CMD20	K25	FB_CMD20	
FB_CMD21	K24	FB_CMD21	
FB_CMD22	F27	FB_CMD22	
FB_CMD23	K27	FB_CMD23	
FB_CMD24	G26	FB_CMD24	
FB_CMD25	B27	FB_CMD25	
FB_CMD26	N24	FB_CMD26	

FB_DQM0	D21	FBDQM0	
FB_DQM1	F22	FBDQM1	
FB_DQM2	F20	FBDQM2	
FB_DQM3	A21	FBDQM3	
FB_DQM4	V27	FBDQM4	
FB_DQM5	W22	FBDQM5	
FB_DQM6	V22	FBDQM6	
FB_DQM7	V24	FBDQM7	

read strobe

FB_DQS_RN0	A22	FBDQS#0	
FB_DQS_RN1	E22	FBDQS#1	
FB_DQS_RN2	F21	FBDQS#2	
FB_DQS_RN3	B21	FBDQS#3	
FB_DQS_RN4	V26	FBDQS#4	
FB_DQS_RN5	W23	FBDQS#5	
FB_DQS_RN6	V23	FBDQS#6	
FB_DQS_RN7	W27	FBDQS#7	

write strobe

FB_DQS_WP0	B22	FBDQS0	
FB_DQS_WP1	D22	FBDQS1	
FB_DQS_WP2	E21	FBDQS2	
FB_DQS_WP3	C21	FBDQS3	
FB_DQS_WP4	V25	FBDQS4	
FB_DQS_WP5	W24	FBDQS5	
FB_DQS_WP6	U24	FBDQS6	
FB_DQS_WP7	W26	FBDQS7	

FBVTT_01	E15	FBVTT	
FBVTT_02	F15		
FBVTT_03	F16		
FBVTT_04	J17		
FBVTT_05	J18		
FBVTT_06	L19		
FBVTT_07	N19		
FBVTT_08	R19		
FBVTT_09	U19		
FBVTT_10	W19		

FBVDDQ_01	F17	FBVDDQ	
FBVDDQ_02	F19		
FBVDDQ_03	J19		
FBVDDQ_04	M19		
FBVDDQ_05	T19		
FBVDDQ_06	J22		
FBVDDQ_07	L22		
FBVDDQ_08	P22		
FBVDDQ_09	U22		
FBVDDQ_10	Y22		

FB_CLK0	L24	(21) FB_CLK0	
FB_CLK0#	K23	(21) FB_CLK0#	
FB_CLK1	M22	(21) FB_CLK1	
FB_CLK1#	N22	(21) FB_CLK1#	
FB_REFCLK	M23	T11 PAD	
FB_REFCLK#	M24	T12 PAD	
FB_DEBUG	K22	T13 PAD	
FB_VREF	A16	FBVREF	
FB_PLLVDD	D14	T52 PAD	
FB_PLLAVDD	D13	FB_PLLAVDD	
FB_PLLAGND	C15		
FBCAL_PD_VDDQ	D15	FBCAL_PD_VDDQ	
FBCAL_PU_GND	E13	FBCAL_PU_GND	
FBCAL_TERM_GND	H22	FBCAL_TERM_GND	

G72M

U31D

Part 4 of 4

GND

B2	GND_01	GND_48	P14
E2	GND_02	GND_49	R14
H2	GND_03	GND_50	U14
L2	GND_04	GND_51	W14
P2	GND_05	GND_52	AC14
U2	GND_06	GND_53	AD14
Y2	GND_07	GND_54	N15
AC2	GND_08	GND_55	P15
AE2	GND_09	GND_56	R15
AF3	GND_10	GND_57	AF15
B5	GND_11	GND_58	N16
E5	GND_12	GND_59	P16
L5	GND_13	GND_60	R16
P5	GND_14	GND_61	AD16
U5	GND_15	GND_62	B17
Y5	GND_16	GND_63	E17
AC5	GND_17	GND_64	L17
H6	GND_18	GND_65	P17
AF6	GND_19	GND_66	U17
B8	GND_20	GND_67	AD17
E8	GND_21	GND_68	AF18
AD8	GND_22	GND_69	K19
K9	GND_23	GND_70	P19
P9	GND_24	GND_71	V19
V9	GND_25	GND_72	AD19
AD9	GND_26	GND_73	B20
AF9	GND_27	GND_74	E20
B11	GND_28	GND_75	AD20
E11	GND_29	GND_76	AF21
F11	GND_30	GND_77	B23
L11	GND_31	GND_78	E23
P11	GND_32	GND_79	H23
U11	GND_33	GND_80	L23
AD11	GND_34	GND_81	P23
N12	GND_35	GND_82	U23
P12	GND_36	GND_83	Y23
R12	GND_37	GND_84	AC23
AD12	GND_38	GND_85	AF24
AF12	GND_39	GND_86	B26
N13	GND_40	GND_87	E26
P13	GND_41	GND_88	H26
R13	GND_42	GND_89	L26
B14	GND_43	GND_90	P26
E14	GND_44	GND_91	U26
J14	GND_45	GND_92	Y26
L14	GND_46	GND_93	AC26
N14	GND_47	GND_94	AF26

G72M

+1.8VRUN
R341 1K/F
FBVREF
R342 1K/F
C624 0.1u/10V

FBVREF = FBVDDQ * Rb/(Rt + Rb).
VREF = 0.5 * FBVDDQ.
DDR: 0.9V = 1.8V * 1K/(1K + 1K).

+1.2V_GFX_PCIE
L7 BLM11A121S
C135 4.7u/6.3V_6
C141 1u/10V
C138 0.01u/16V

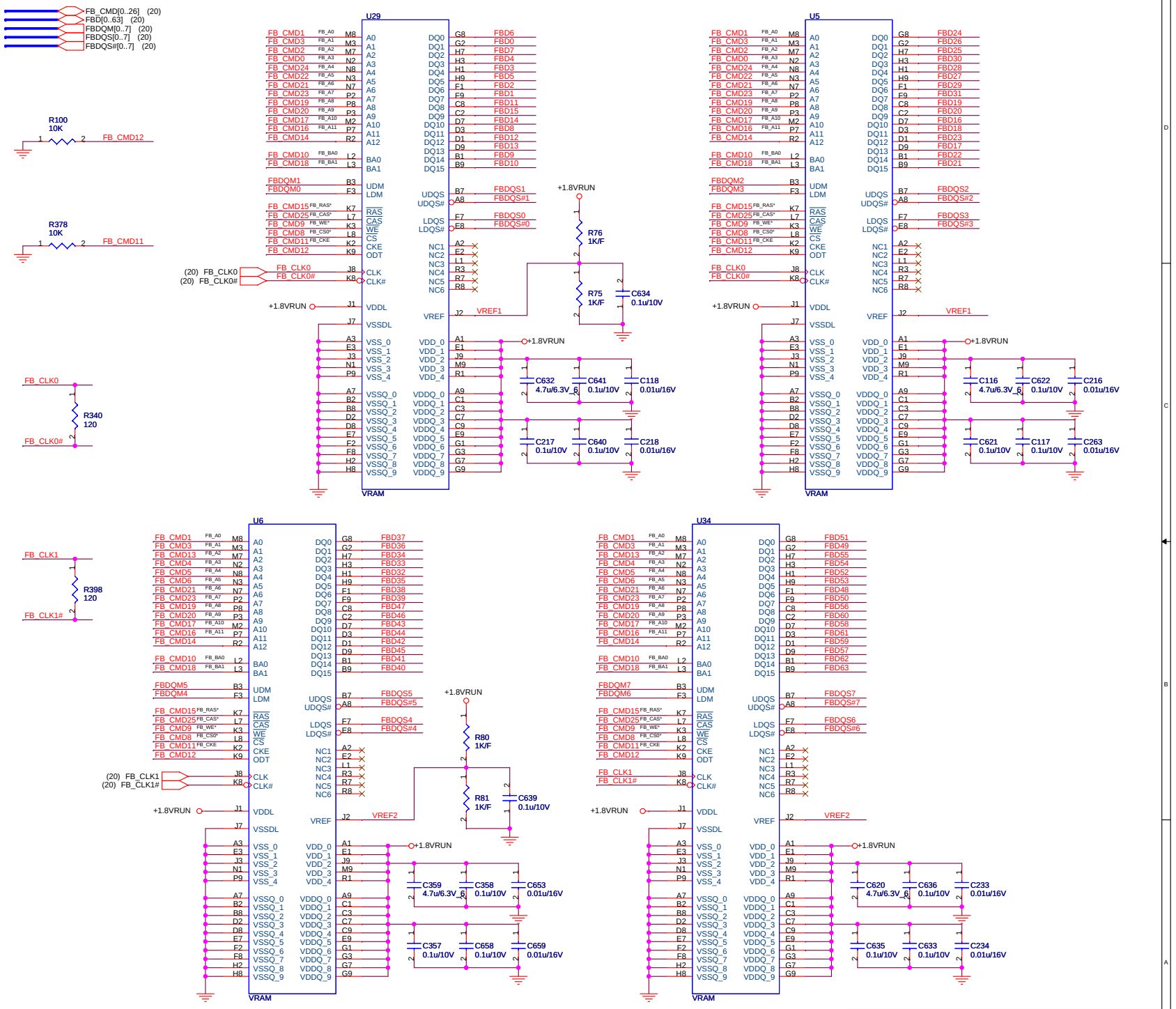
+1.8VRUN
R53 40.2/F
R57 *0
R52 30/F

PLACE BELOW GPU

+1.8VRUN
C179 4700p/25V
C213 0.022u/16V
C232 0.1u/10V
C130 4700p/25V
C638 0.1u/10V
C661 4.7u/6.3V_6
C650 1u/10V
C177 4700p/25V
C191 0.022u/16V
C251 0.1u/10V
C180 4700p/25V
C214 0.022u/16V
C252 0.1u/10V
C235 4.7u/6.3V_6
C157 4700p/25V
C166 0.022u/16V
C172 0.1u/10V
C190 0.022u/16V
C158 0.1u/10V
C630 1u/10V

PROJECT : TW3
Quanta Computer Inc.

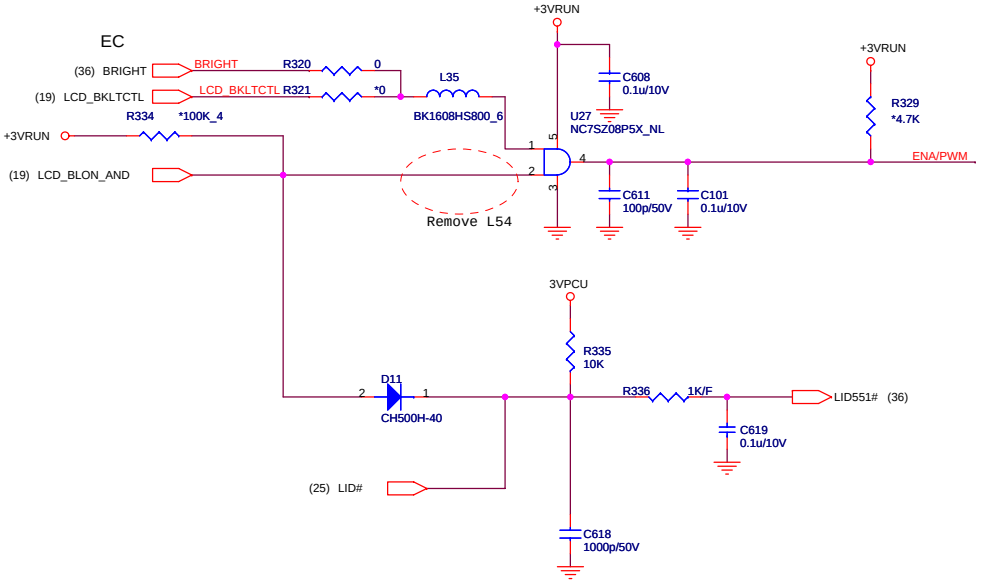
Size	Document Number	Rev
	NV72M-3	3A
Date: Thursday, June 15, 2006	Sheet 20 of 48	

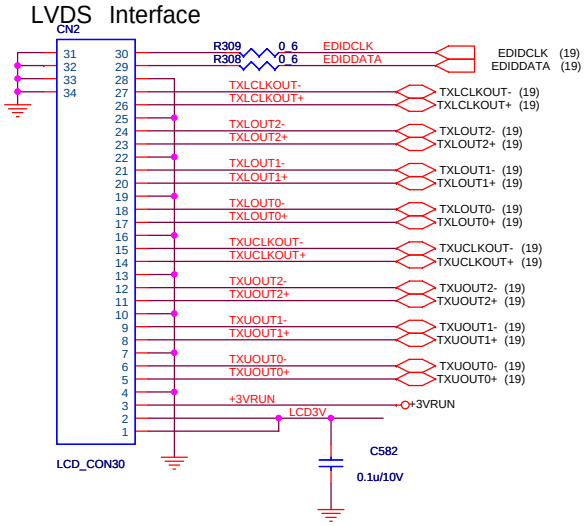


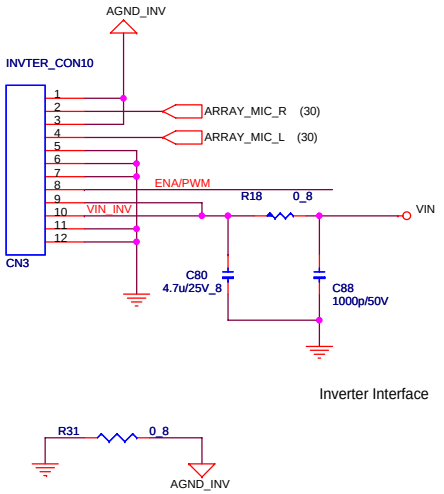
PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	NV72M-4	3A

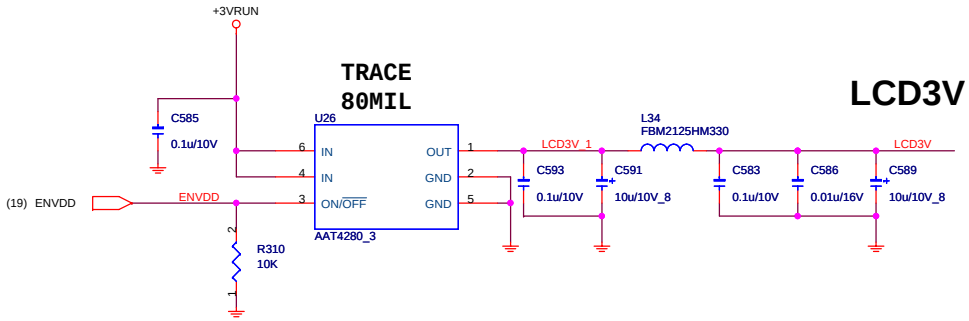
Date: Thursday, June 15, 2006 Sheet 21 of 48







Inverter Interface



PROJECT : TW3 Quanta Computer Inc.		
Size	Document Number LCD,INVERTER CONN	Rev 3A
Date: Thursday, June 15, 2006	Sheet 22 of 48	

CRT PORT

NI for DVI

2/22 Tony Huang

ESD PROTECTION

CM2009

CRT	R150,R159	Q37,Q38	RP56
DVI	R150,R160	Q37,Q39	RP56

add GPU's I2CA stuff option to TMDS I2C pin if design DVI-I (CRT + TMDS).

2/22 Tony Huang

CRT SWITCH

SEL	FUNCTION(COM)
LOW	IN_B0
HIGH	IN_B1

DVI DETECT

Install for DVI

3/9 Tony

5/10 Tony

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	CRT,TV-OUT,DVI CONN.	3B

Date: Thursday, June 15, 2006 Sheet 23 of 48

C: 88E8053 LF PN: AJ080530010 (20050414)

1Mbits

C: Add 9 X GND Pad for LAN controller. (20050411)

C: Add these GND pin for via hole to GND Plane.

C: Add RC (R37 change to 200K, Add C101) delay to control LOM_DISABLE#. (20050411)

C: Reserve R36. Change LANRST# to PCIRST# source from MB option modify.(2005/04/11)

CLOSE CHIP

DELAY PIN10 AT LEAST 150ms

88E8038/88E8055

FOR 8038	
R389	2K
R9	NC

Install for 8038

NI for 8038

LANVCC

PLACEMENT CLOSE TO EACH OTHER

C: Widen to 20 mils. AVDD25 to 20 mils.(20050411)

C: Widen to 20 mils. VDD to 20 mils.(20050411)

0804 REDUCING THE LANVCC NOISE

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Marvell 88E8036,88E8053	3A

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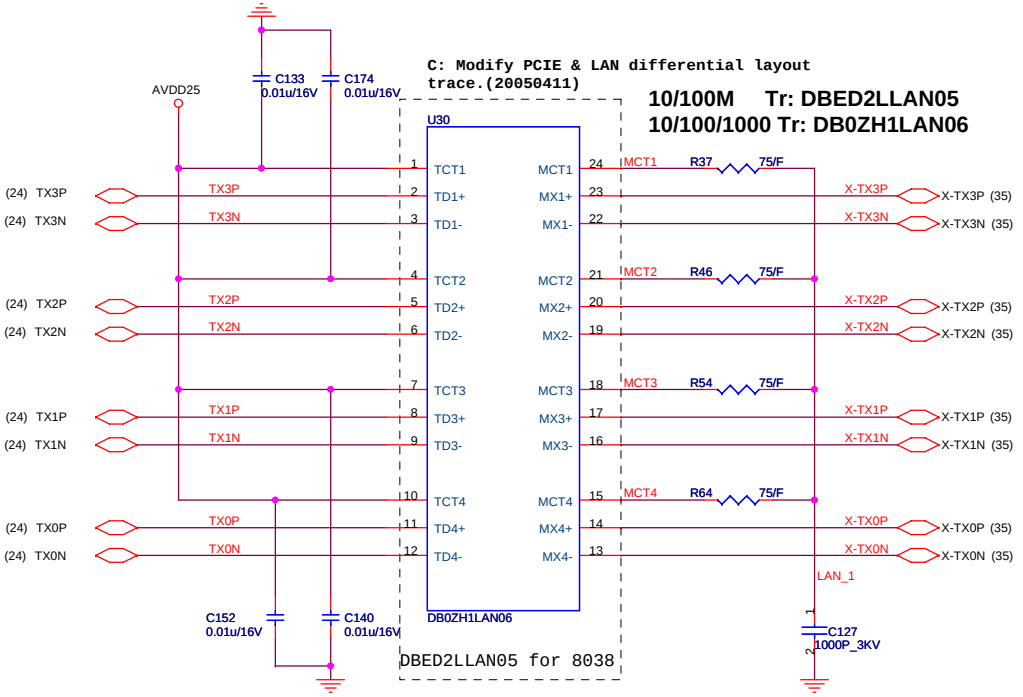
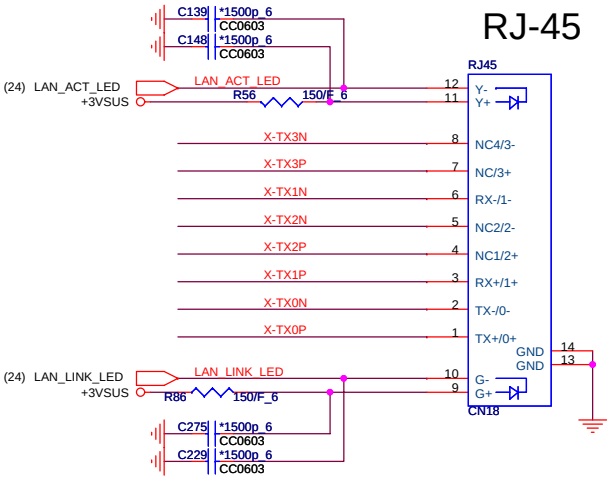
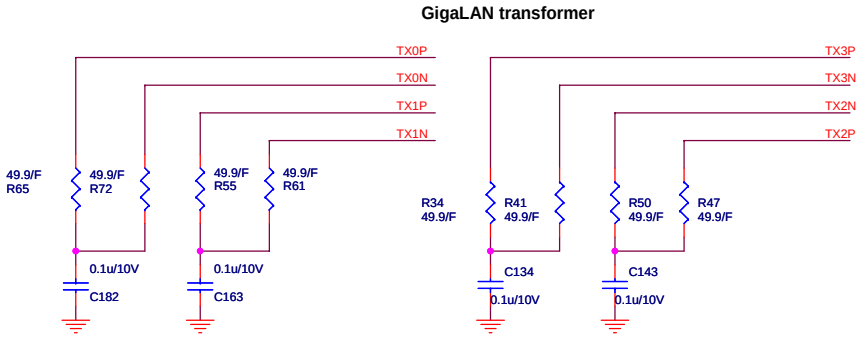
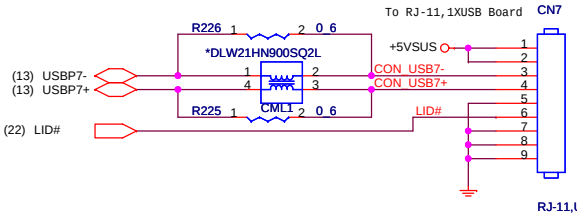


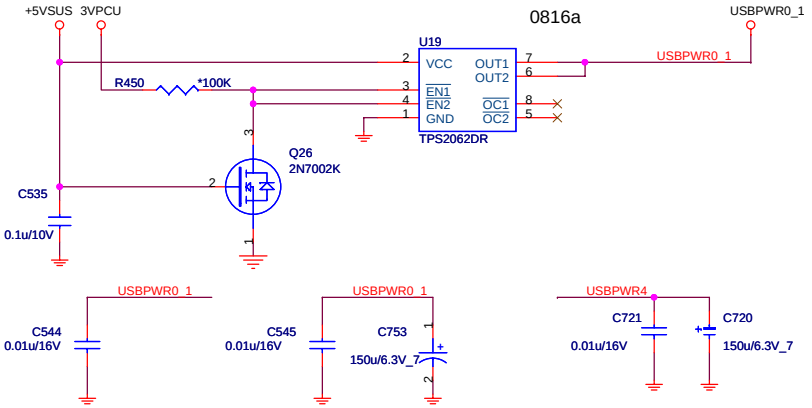




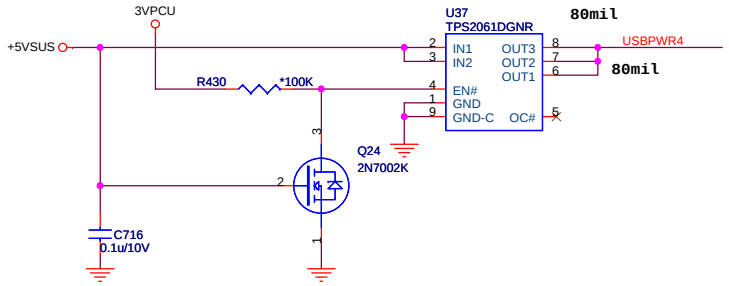


PROJECT : TW3
Quanta Computer Inc.

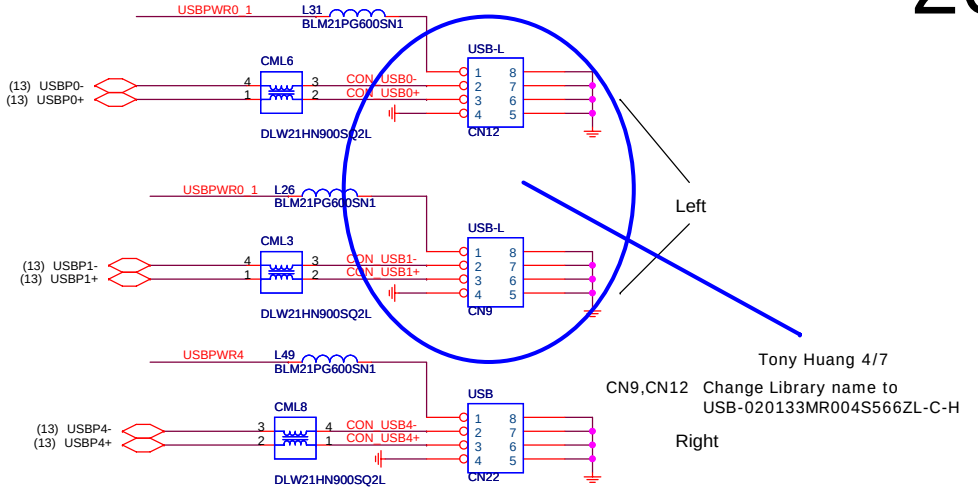
Size	Document Number	Rev
	LAN SW CONN& MDC CONN	3A
Date: Thursday, June 15, 2006	Sheet 25 of 48	



C:Change U1 from G528 to TPS2061



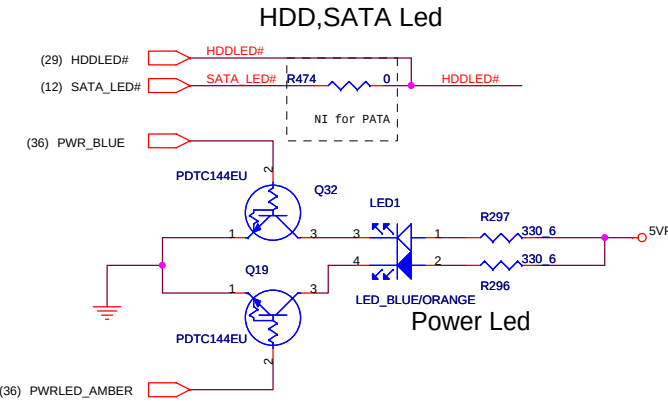
USB Port

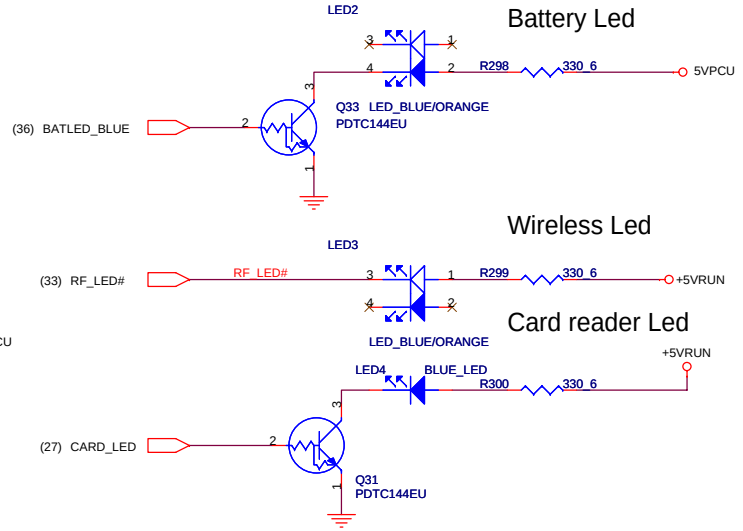


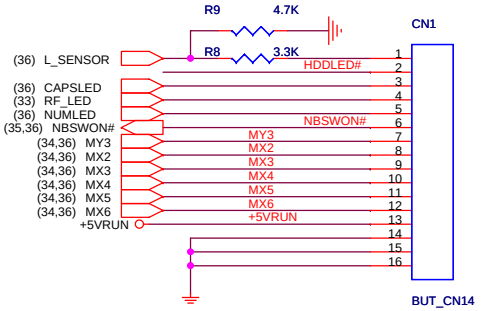
Tony Huang 4/7

CN9,CN12 Change Library name to USB-020133MR004S566ZL-C-H

For Botton Board

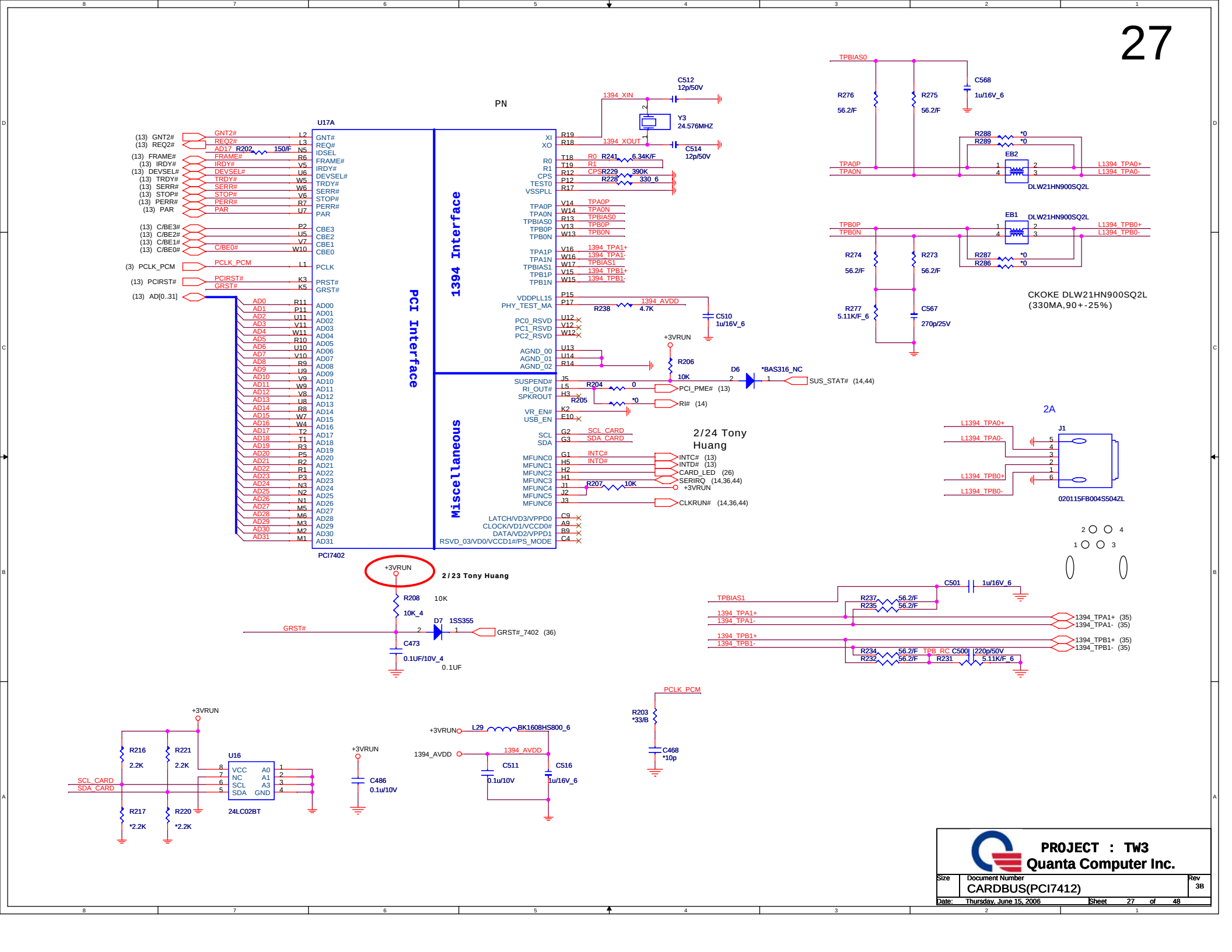






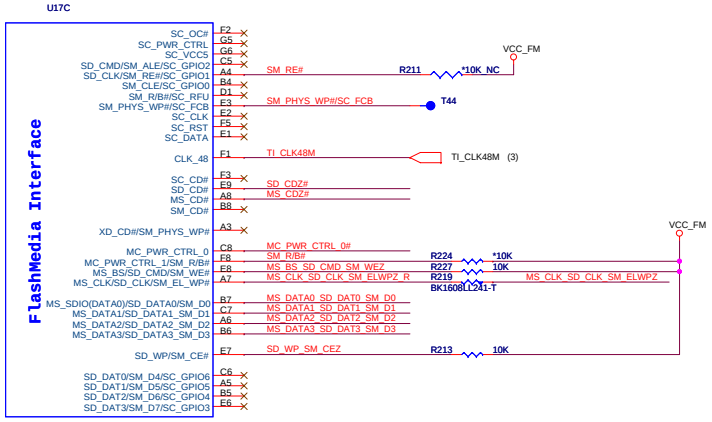
PROJECT : TW3
Quanta Computer Inc.

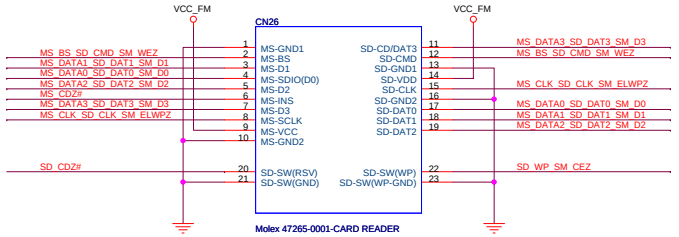
Size	Document Number	Rev
	USB,LED,Buttom/B	3B
Date: Thursday, June 15, 2006	Sheet 26 of 48	


PN
U17A
PCI7402
PCI Interface
1394 Interface
Miscellaneous
2/24 Tony Huang
2/23 Tony Huang
CKOKE DLW21HN900SQ2L
(330MA,90+-25%)
2A
J1
020115FB004S504ZL
DLW21HN900SQ2L
24LC02BT
U16
Y3
24.576MHZ
BK1608HS800_6
D6
*BAS316_NC
D7
1SS355
EB1
EB2

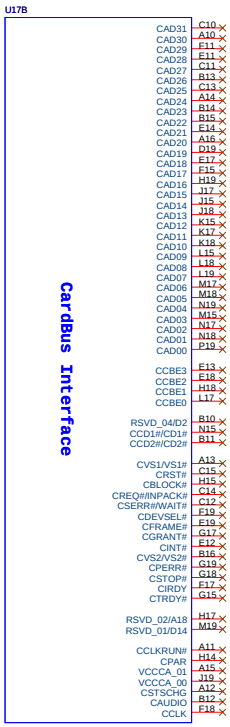
DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

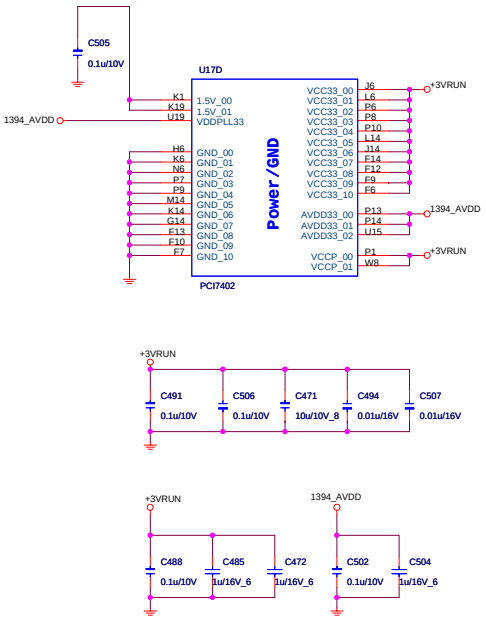
3 IN1 CARD READER (push-push)

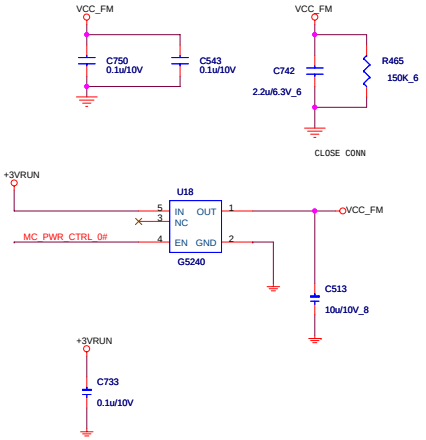




Supporting MMC/SD/MS Cards
Molex P/N:DFHD23MS0B6



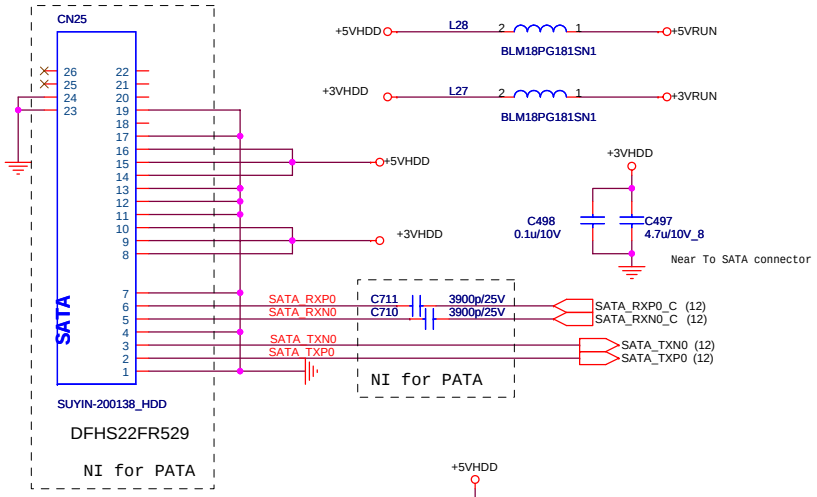


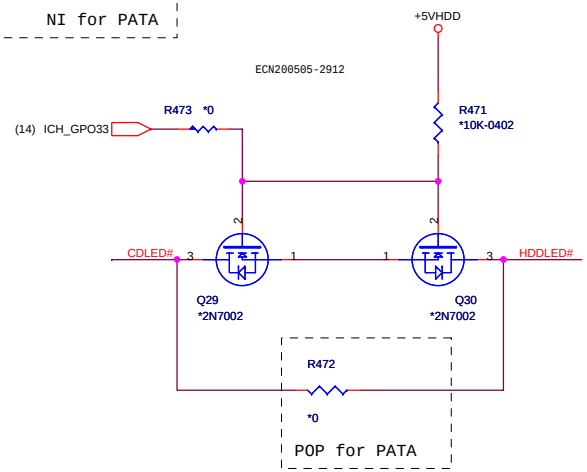


PROJECT : TW3
Quanta Computer Inc.

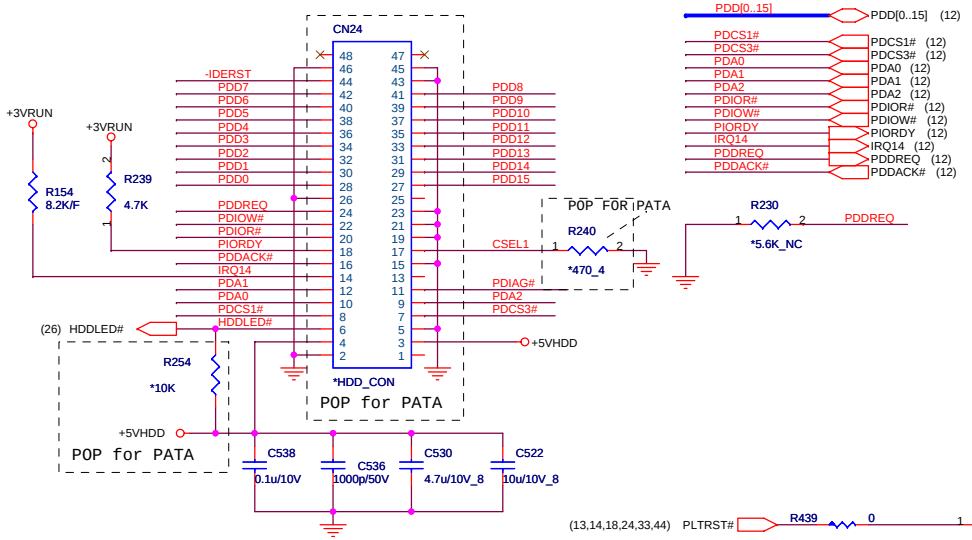
Size	Document Number	Rev
	1394 CONTROLLER	3A
Date: Thursday, June 15, 2006	Sheet 28 of 48	

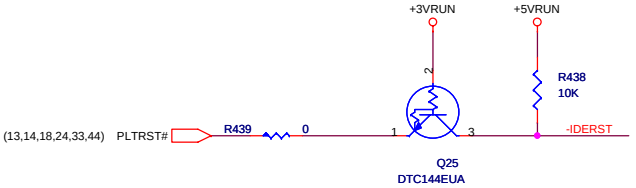
SATA HDD



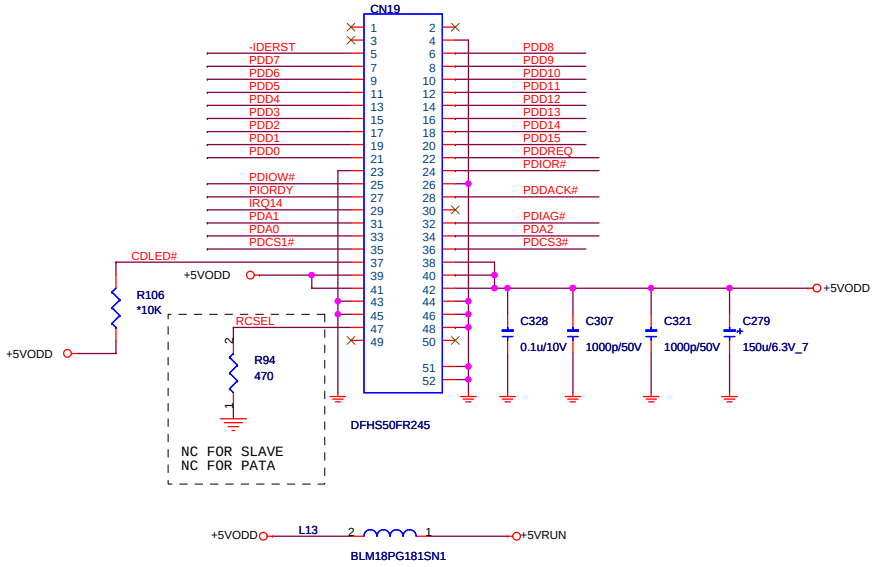


PATA HDD





ODD



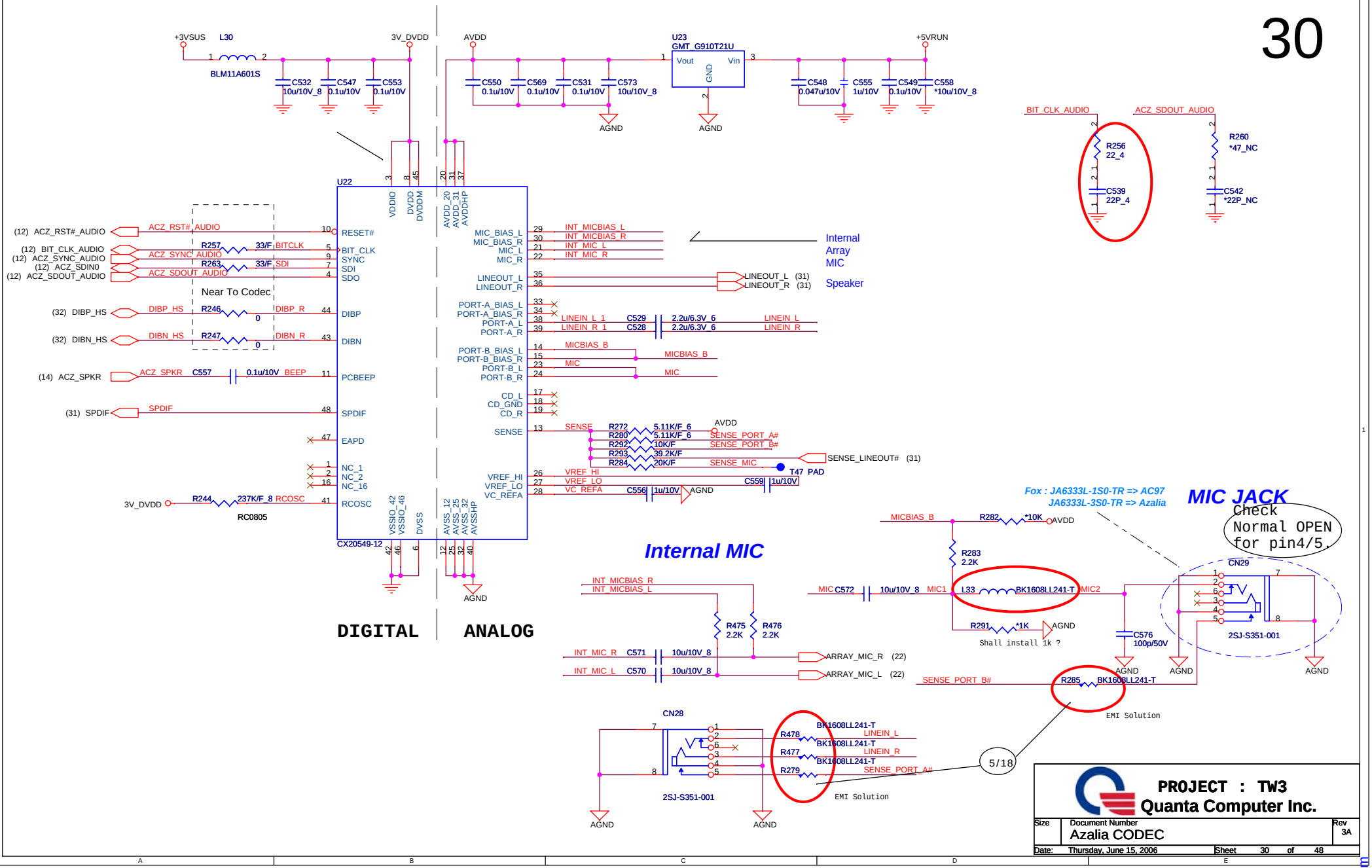
FOR PATA HDD

CN19	NI
C730	NI
C729	NI
CN18	HDD CON
R517	NI
Q25	2N7002
Q26	2N7002
R513	10K
R512	0
R168	470

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	SATA,PATA(HDD,ODD)	3B

Date: Thursday, June 15, 2006 Sheet 29 of 48



PROJECT : TW3			
Quanta Computer Inc.			
Size	Document Number		Rev
	Azalia CODEC		3A
Date: Thursday, June 15, 2006		Sheet 30 of 48	

Modify Library to QFN28-5X5-5-33P(Add thermal Pad) 04/06/2006 by Tony Huang

04062006

EAPD
low:mute

HEADPHONE OUT/SPDIF

GAIN	SPKR MODE	HP MODE
0	10.5	3
1	9	0

New add Pin29~31

Check Normal OPEN for pin4/5.

SPEAKER CON. BK1608HM121

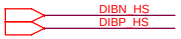
3 / 9 Tony Huang

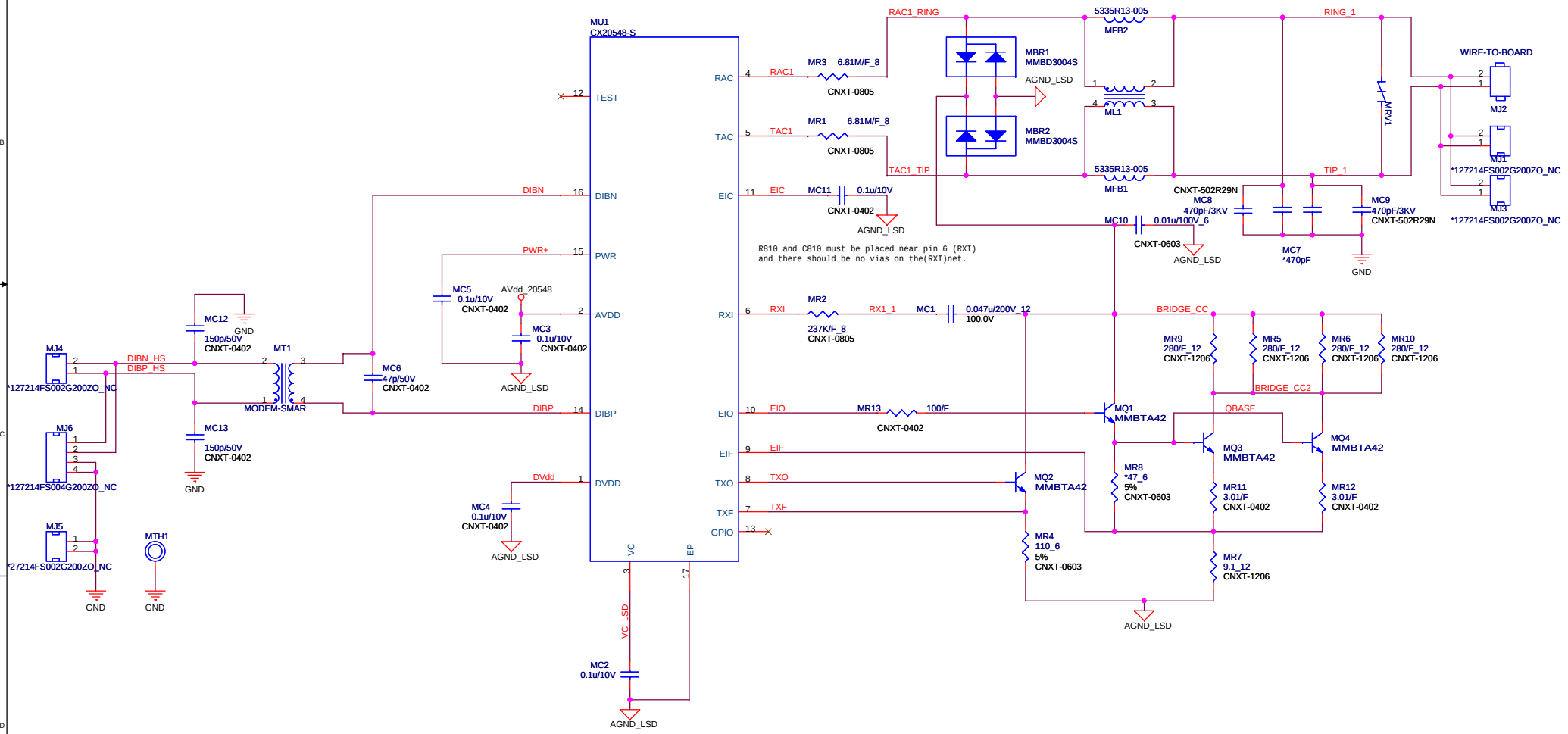
When Docking insert , disable BTL

PROJECT : TW3 Quanta Computer Inc.		
Size	Document Number: AUDIO AMPLIFIER	Rev: 3A
Date: Thursday, June 15, 2006	Sheet 31 of 48	

Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005

(30) DIBN_HS
(30) DIBP_HS

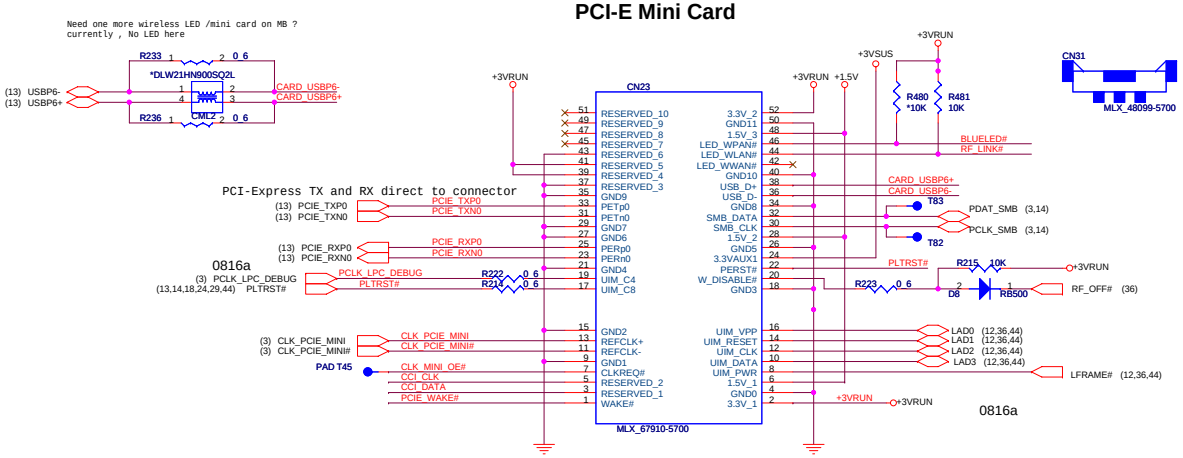




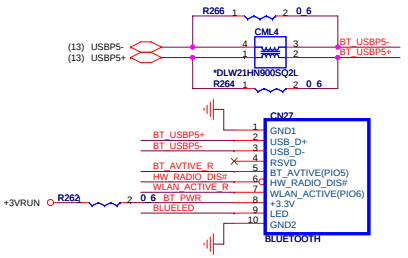
PROJECT : TW3
Quanta Computer Inc.

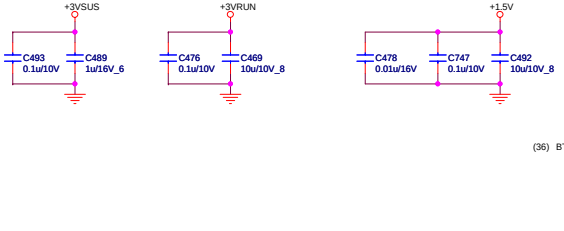
Size	Document Number	Rev
	Conexant Modem	3B
Date: Thursday, June 15, 2006	Sheet 32 of 48	

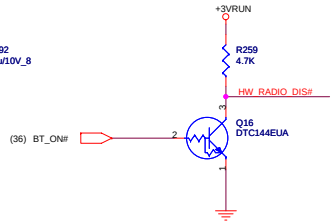
PCI-E Mini Card

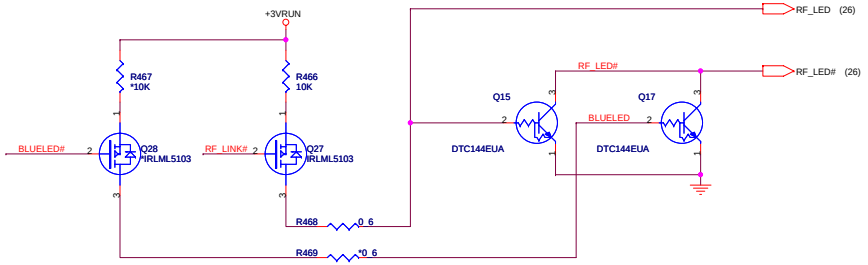


BLUETOOTH CONNECTOR

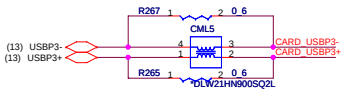


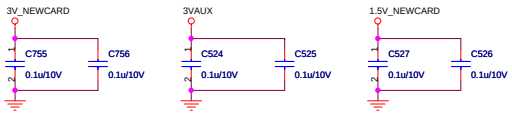


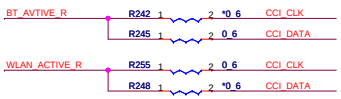


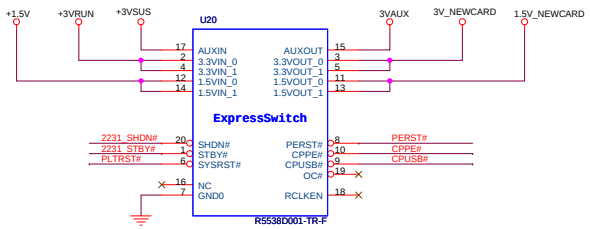


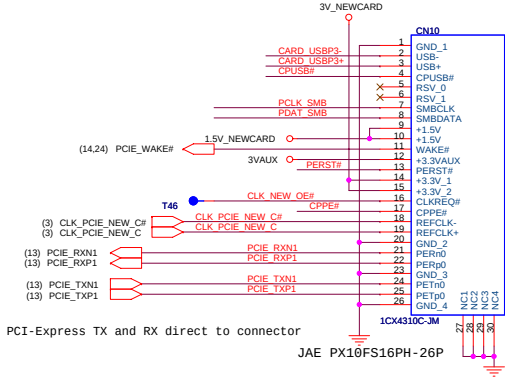
NEWCARD (PCIEXPRESS*1 + USB*1)









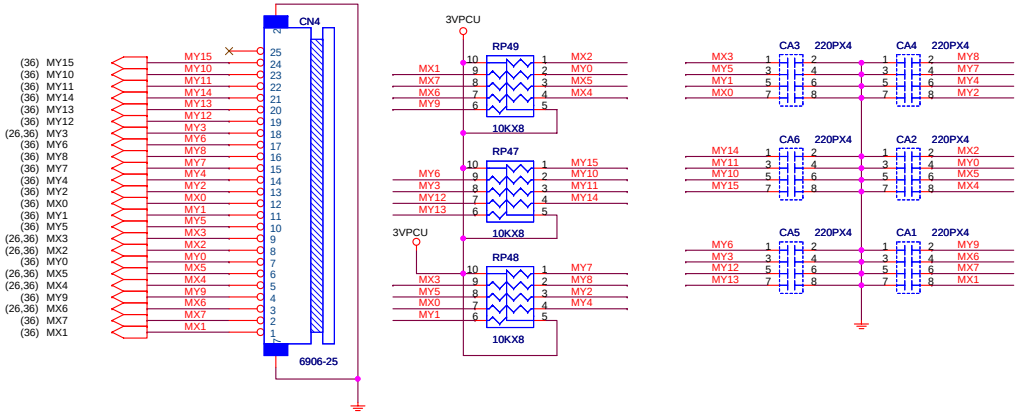


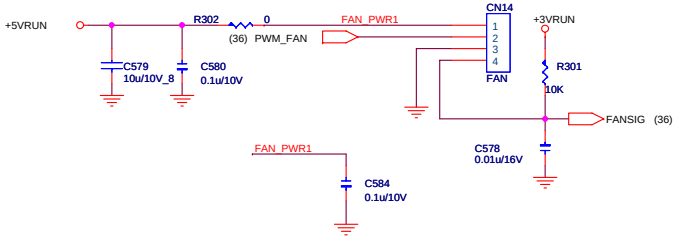
PROJECT : TW3
Quanta Computer Inc.

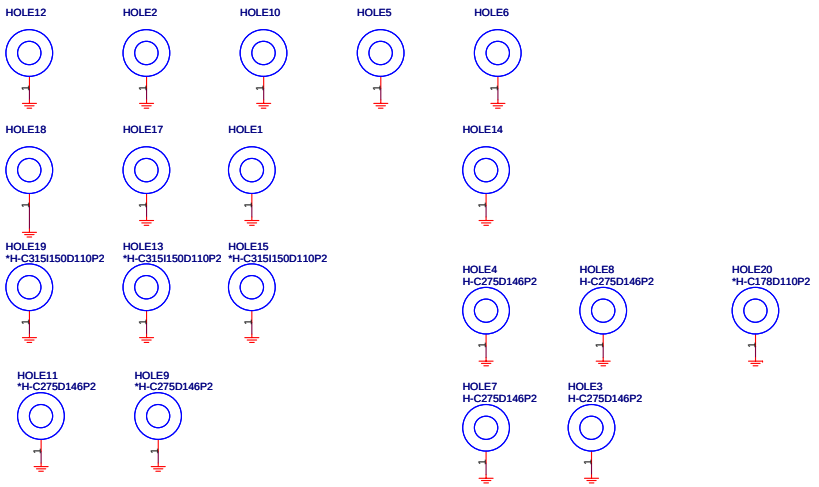
Size	Document Number	Rev
	BT,NEW CARD,MINI PCIE	3B

Date: Thursday, June 15, 2006 Sheet 33 of 48

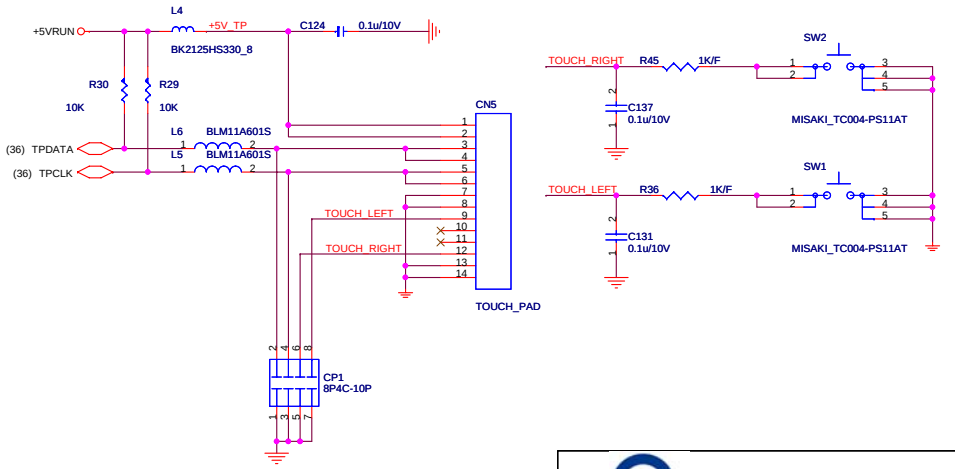
KeyBoard Interface







TOUCH PAD

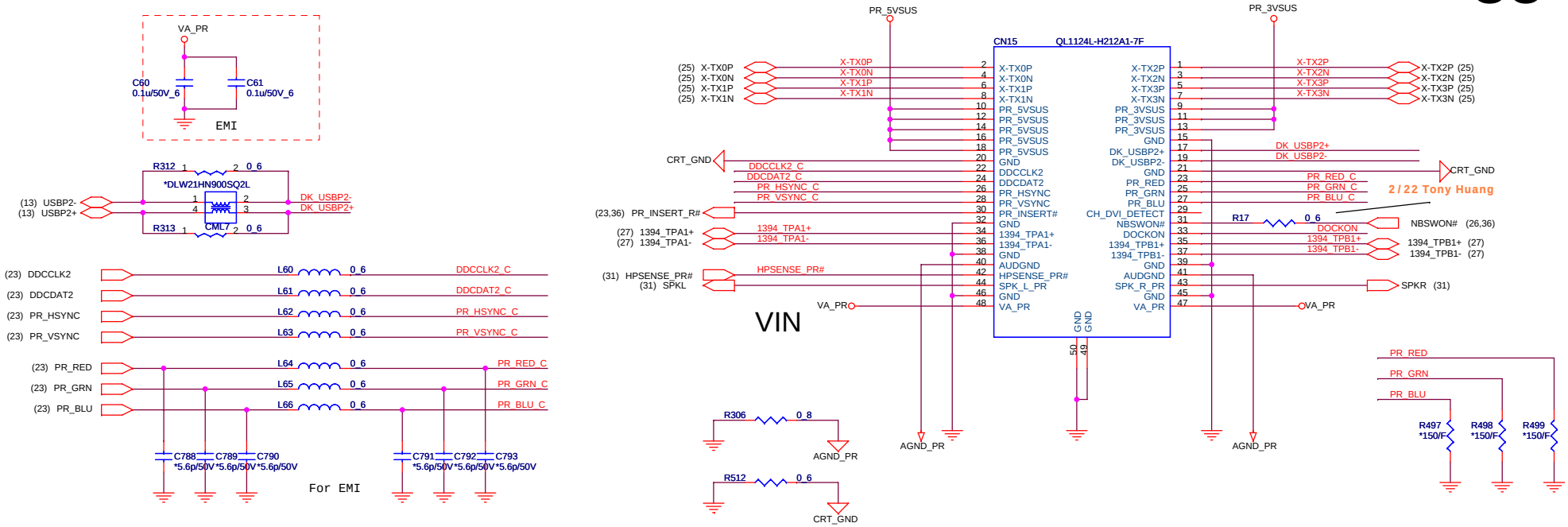


PROJECT : TW3
Quanta Computer Inc.

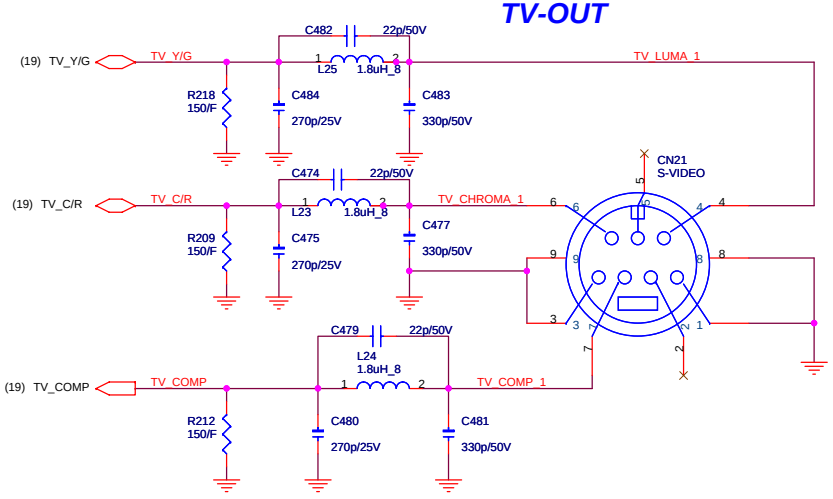
Size	Document Number	Rev
	T/P,FAN,KB	3A

Date: Thursday, June 15, 2006 Sheet 34 of 48

CABLE DOCKING CONNECTOR



TV-OUT



CX8PG181001 (180 ohm ,1.5A)

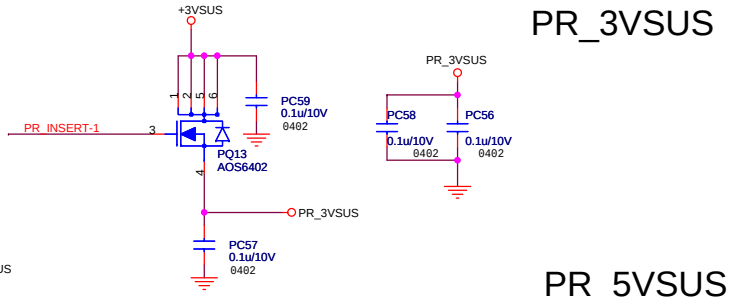
CH00606TB04 CH00606TB04

Intel CRB

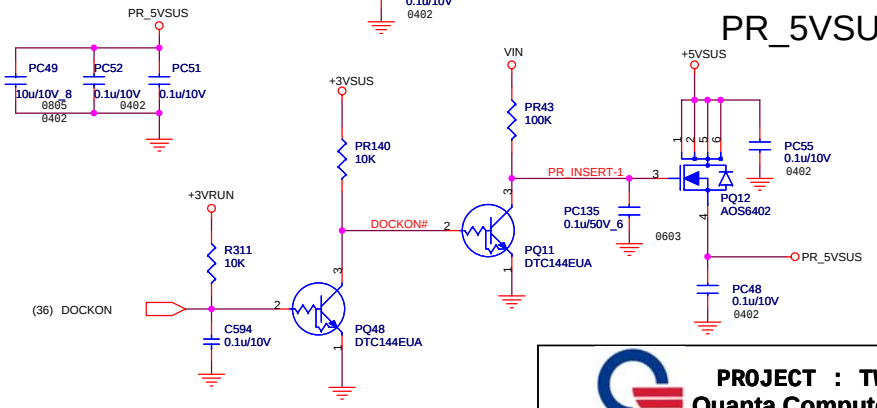
150 ohm@ 100MHZ
(100mA)

6pf 16V 6pf 16V

PR_3VSUS



PR_5VSUS



PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	PORT REPLICATOR	3B
Date: Thursday, June 15, 2006	Sheet 35 of 48	

LDRQ#(pin 8) internal is no use

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

0816a

0816a

PS/2 to Port Replicator

CIRON

Power LED controll

FLASH 8Mbit (1M Byte),NO PLCC TYPE

AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

IOSEL# is NC now

Battery LED BLUE and AMBER

AKE358AKZ61 IC EEPROM(40P)MX29LV008BTTC-70G(1M*8)LF

AKE358AKZ87 IC EEPROM(40P)MX29LV008CTTC-70G(1M*8)LF

1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
2.SIO has internal 20 mS delay of VCC1_PWROK

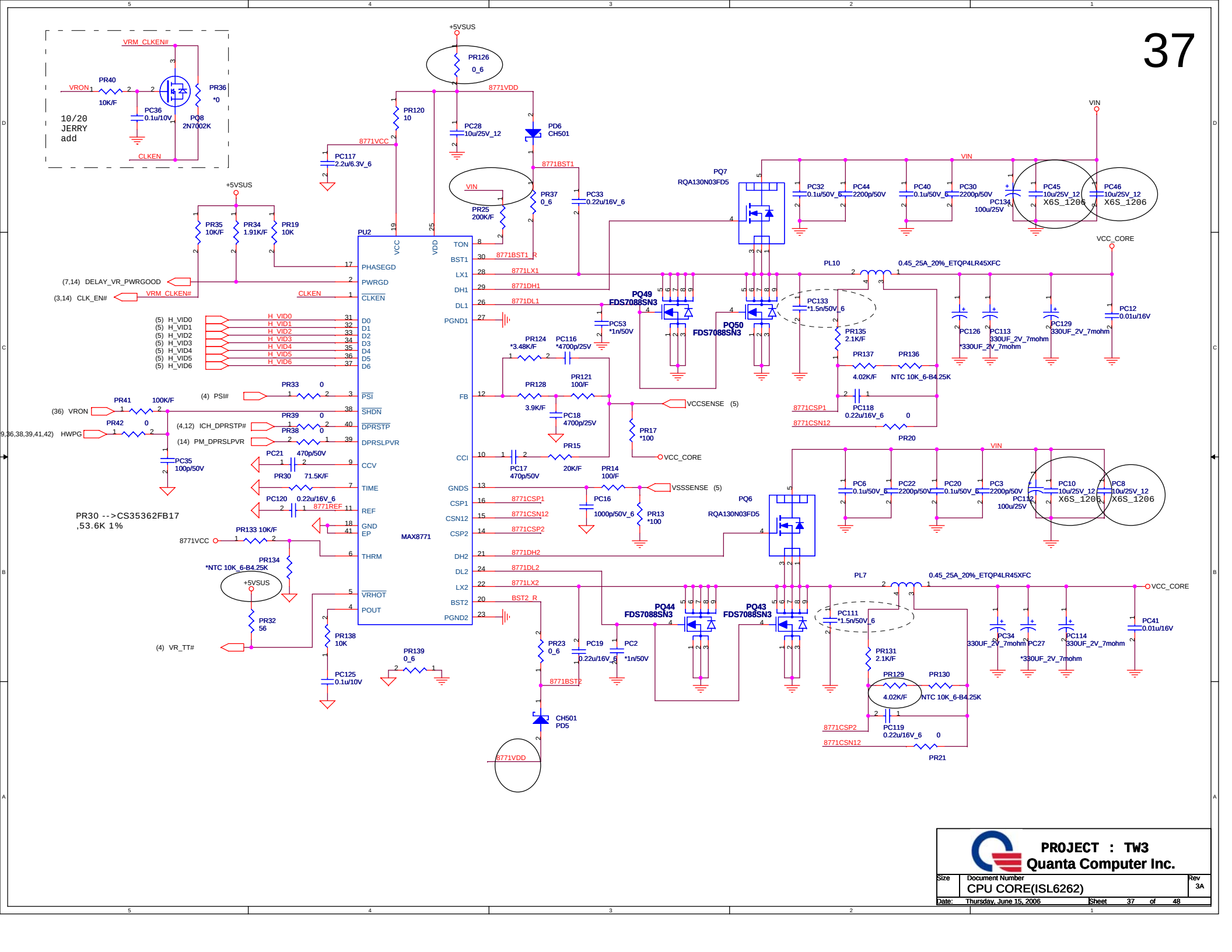
I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

hexamf@hotmail.com

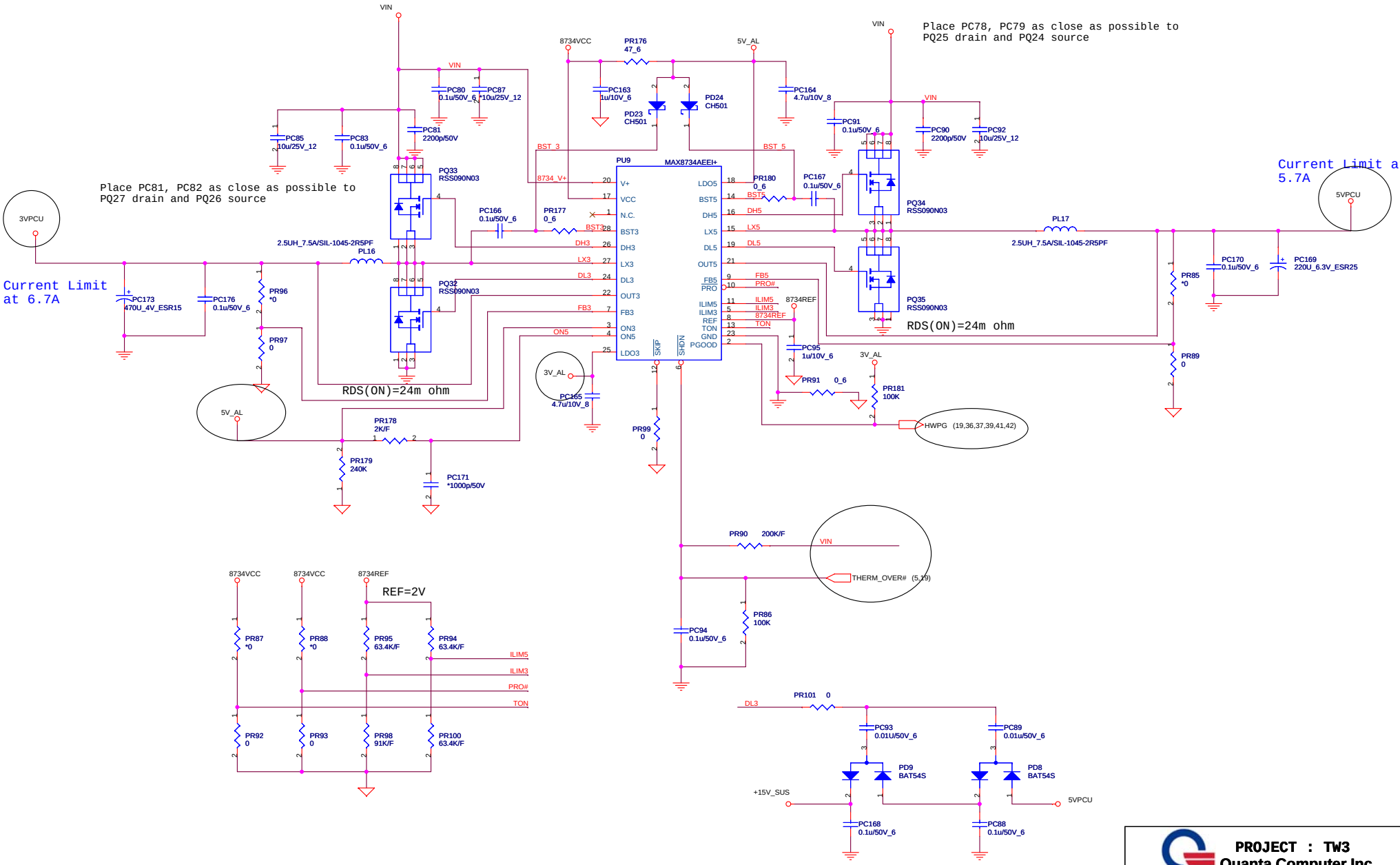
PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	PC87541V & FLASH	3B

Date: Thursday, June 15, 2006 Sheet 36 of 48

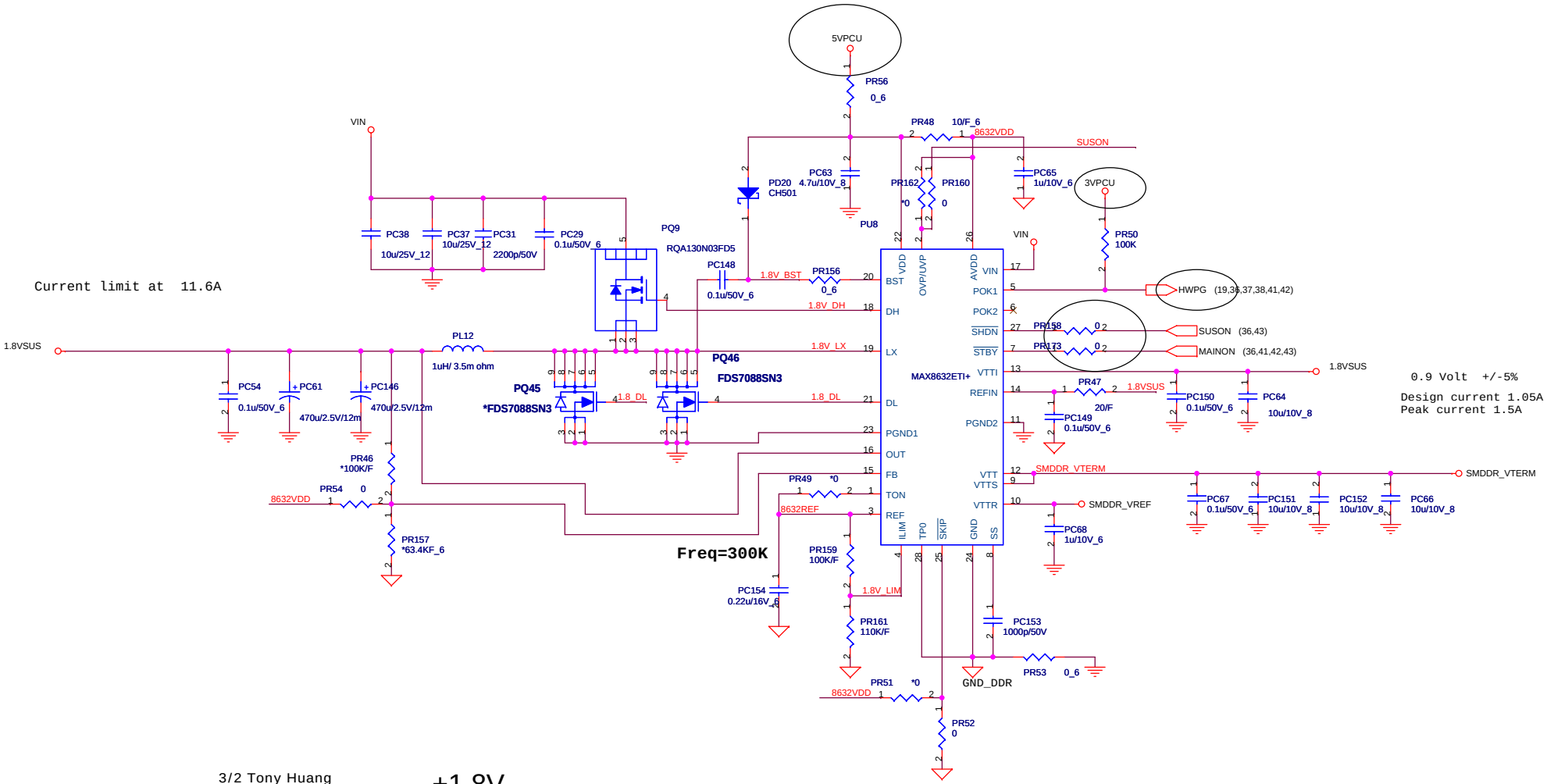


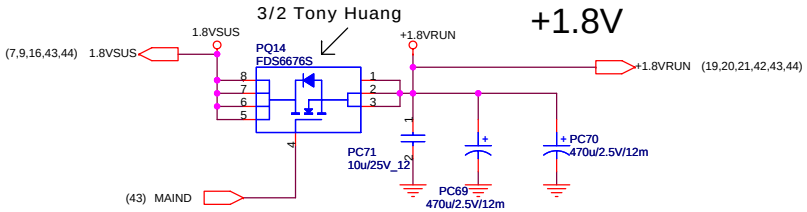
PROJECT : TW3 Quanta Computer Inc.			
Size	Document Number		Rev
	CPU CORE(ISL6262)		3A
Date: Thursday, June 15, 2006		Sheet 37 of 48	



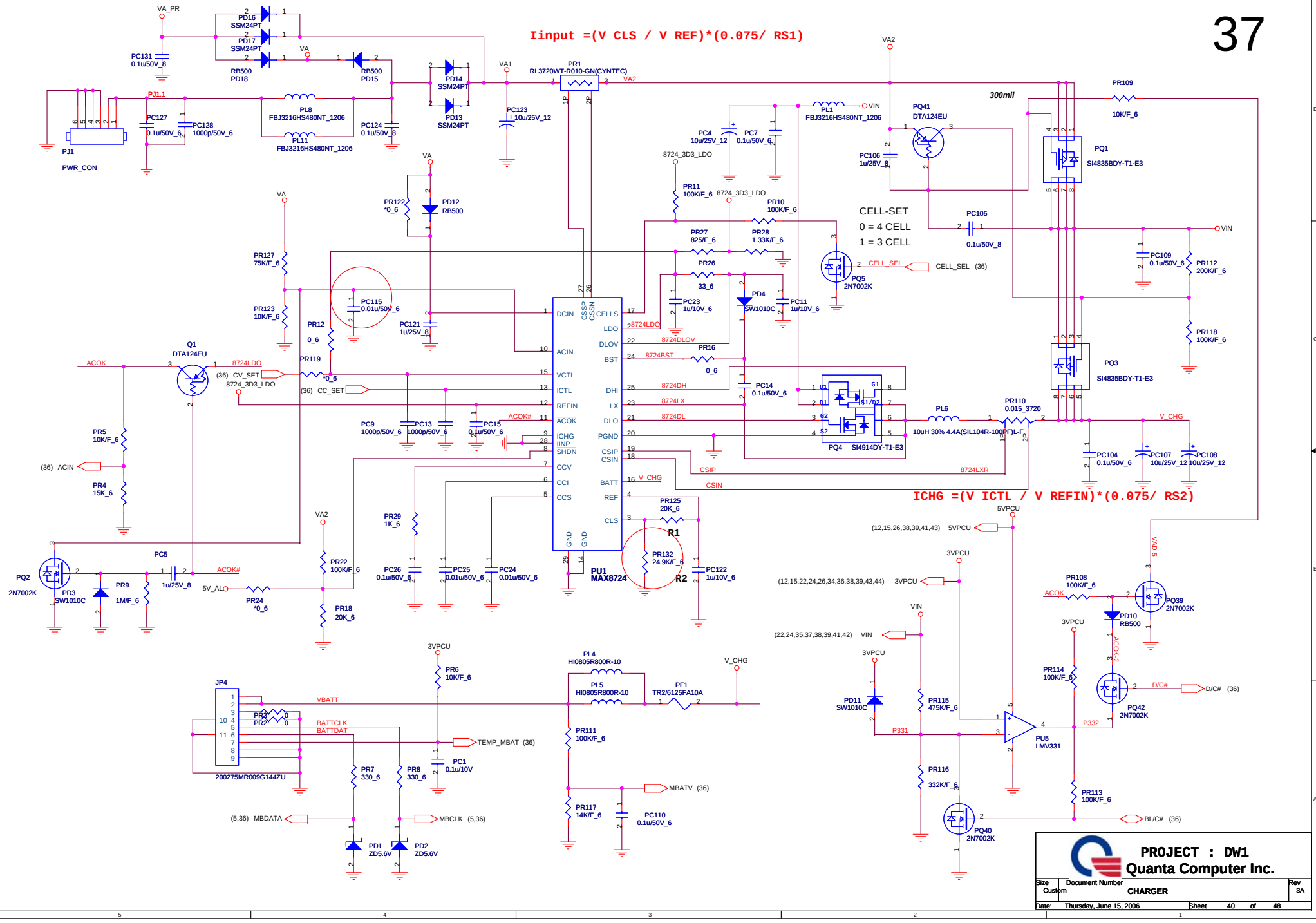
hexainf@hotmail.com

PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number: 5V/3.3V(TPS51120)	Rev: 3A
Date: Thursday, June 15, 2006	Sheet 38 of 48	

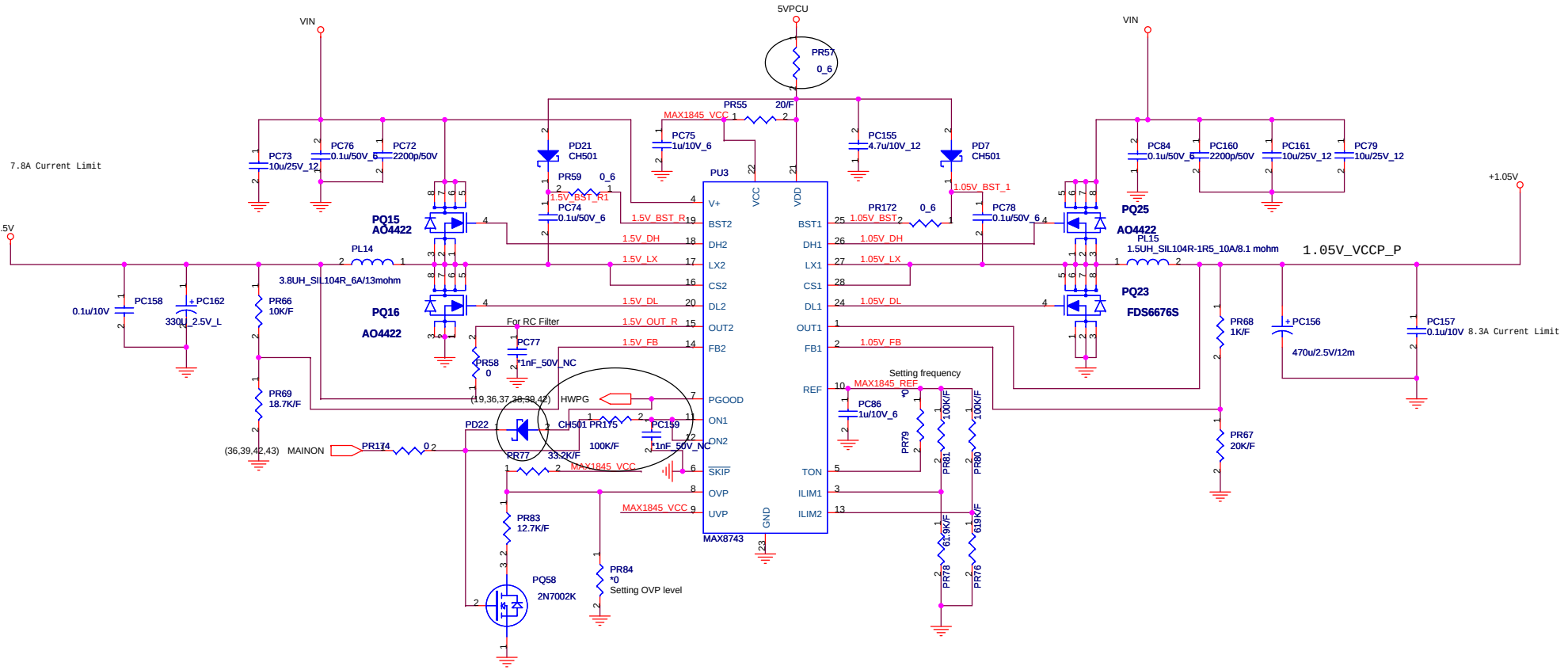




PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number	Rev
	1.8VSUS/+0.9TERM/+2.5VSUS	3A
Date: Thursday, June 15, 2006	Sheet 39 of 48	



AO4422: Id= 11A, Rdson= 24m ohm, Qg= 19.8nC
FDS6676S: Id= 14.5A, Rdson= 7.25m ohm, Qg= 43 nC



PROJECT : TW3			
Quanta Computer Inc.			
Size	Document Number		Rev
	1.05V&1.5V		3B
Date: Thursday, June 15, 2006		Sheet 41 of 48	

(13,14,25,30,33,35,43,44) +3VSUS +3VSUS
(25,26,35,37,43,44) +5VSUS +5VSUS
(22,24,35,37,38,39,40,41) VIN VIN

RQW130N03: Id= 13A, Rdson= 17.1m ohm, Qg= 12.6nC
RQW200N03: Id= 20A, Rdson= 5.6m ohm, Qg= 40 nC

CHOKE: 0.56U +-20% 15A(ETQP4LR56WFC) 1.6m ohm +/-5%

1.0V/ 9.3A/ OCP= 13A

+VCC_GFX_CORE
VIN
VIN_1993
+5VSUS
+3VRUN
PL2 HI0805R800R-10
PC42 10u/25V_12
PC47 10u/25V_12
PC50 0.1u/50V_6
PC39 2200p/50V
PR145 0_6
PR146 20_6
VGA_P_VCC
PD19 CH501
PC60 1u/10V_6
PC142 1u/10V_6
PR154 100K/F
HWPG (19,36,37,38,39,41)
PC144 0.1u/50V_6 3/9 Tony
PR151 0
MAINON (36,39,41,43)
PR147 *0
V_PWRCNTL (19)
VGA_REFIN
VGA_P_REF
PR150 75K
PR45 75K
PR148 20K/F
PC143 470p/50V
PR152 *0
PR155 137K/F_6
PC62 1u/10V_6
PR153 20K/F
PC147 470p/50V
PR144 0
PR44 0_6
PQ10 RQA130N03FD5
PQ47 RQW180N03
PC136 0.1u/50V_6
PC132 0.1u/50V_6
PC43 330U_2V_9m
PC130 330U_2V_9m
PL9 0.56uH/ 1.6m ohm
PR31 1.62K/F
PC138 0.22u/25V_6
1993_DH
1993_LX
1993_DL
1993_CSP
VGA_BST
PR141 0_6
PU6 MAX1993ETG
VDD BST DH LX DL GND CSP CSN OUT FB
OVP/UVP VCC V+ POK LSAT SHDN GATE REFIN OD GND GND GND GND GND TON REF SKIP FBLANK ILIM

V_PWRCNTL:
High(3.3V) = 1.0V
Low(0V) = 1.1V

Iout_max = 13.4A

Tony Huang 3/2

	NV72M:1.1V G72M:	NV72MV:1.0V
PR150	75K	75 K
PR45	75K	75K
PR148	20K	0 ohm
PR147	NC	NC

+1.2V_VPCIE

1.2V/ 2A

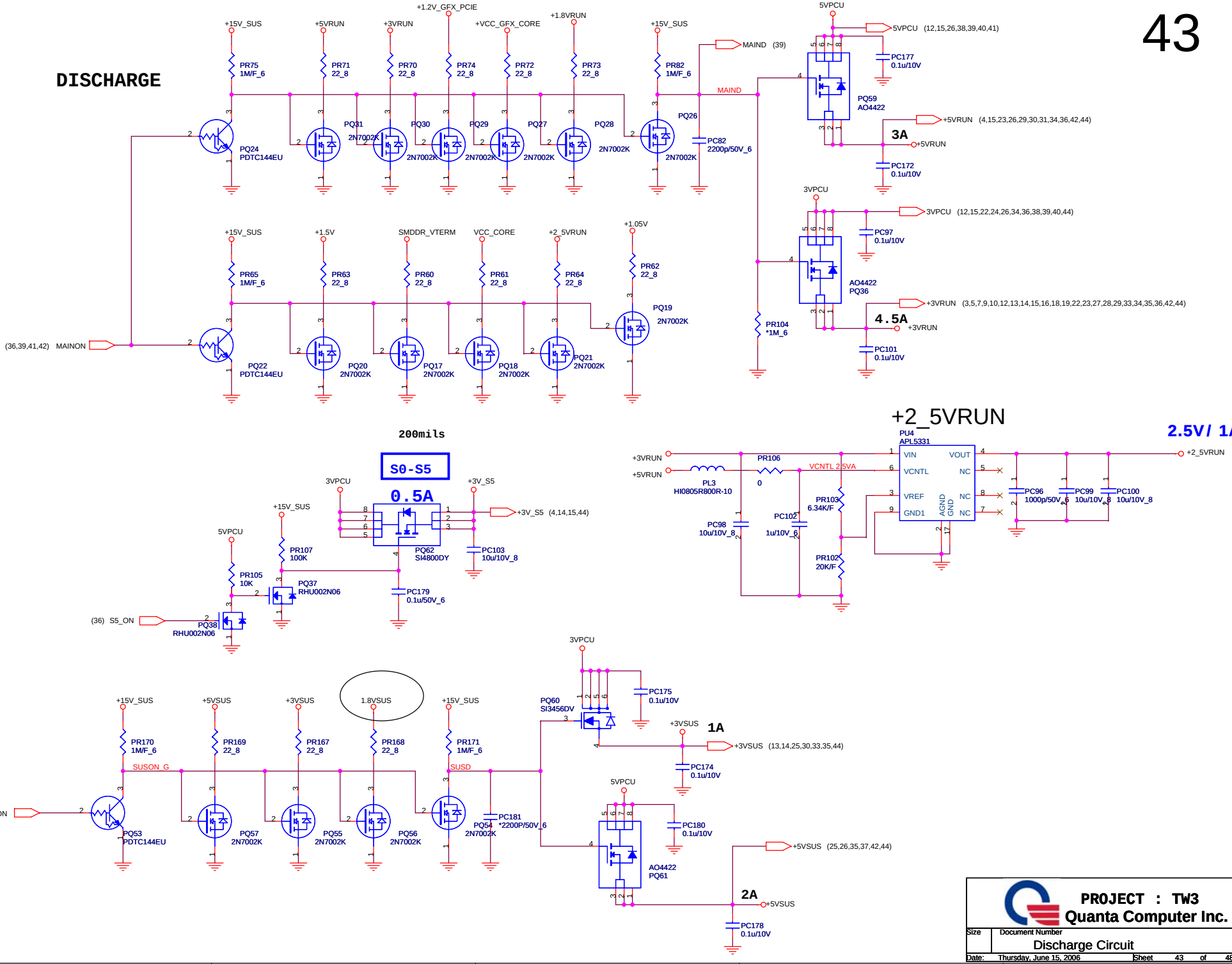
PU7 APL5331
VIN VCNTL VREF GND1 VOUT NC NC NC AGND GND
+1.8VRUN
+5VRUN
PL13 HI0805R800R-10
PR149 0
VCNTL 1.2VA
PR142 10K/F
PR143 20K/F
PC137 10u/10V_8
PC145 1u/10V_6
PC141 1000p/50V_6
PC140 10u/10V_8
PC139 10u/10V_8
+1.2V_GFX_PCIE

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	VGA CORE	3A

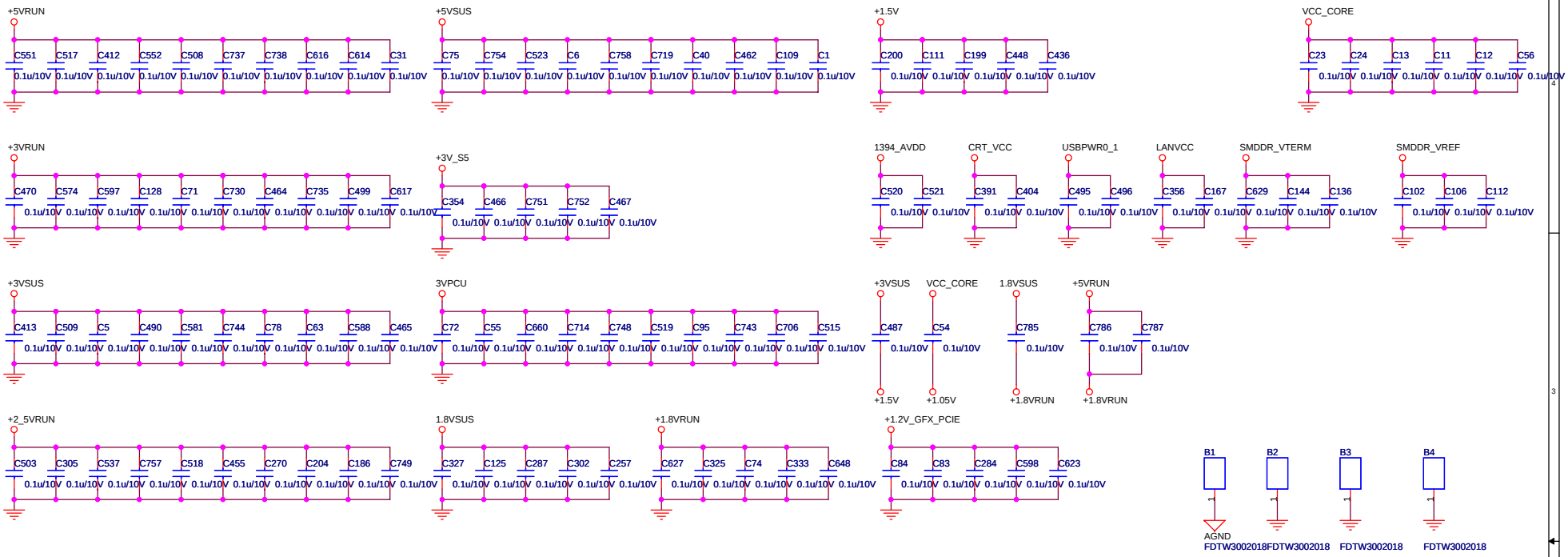
Date: Thursday, June 15, 2006 Sheet 42 of 48

DISCHARGE



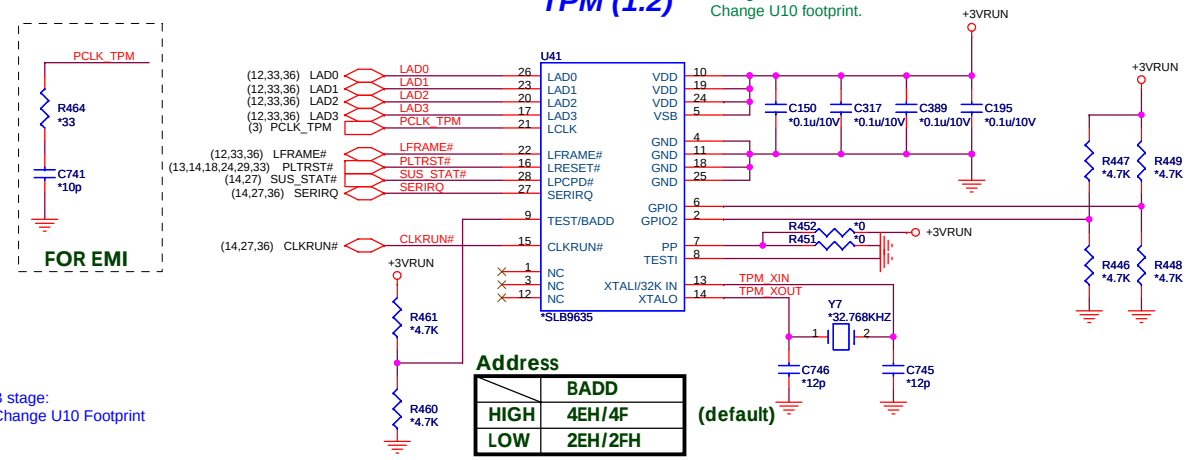
PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge Circuit	3B
Date: Thursday, June 15, 2006	Sheet 43 of 48	



TPM (1.2)

B stage:
Change U10 footprint.



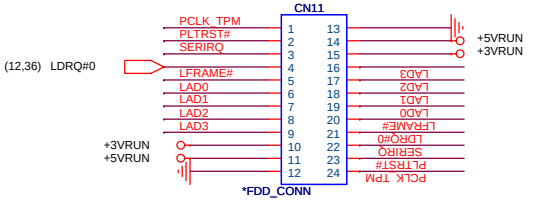
B stage:
Change U10 Footprint

Address

	BADD
HIGH	4EH/4F
LOW	2EH/2FH

(default)

Debug Conn.



PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	EMI & TPM & Debug Conn	3A
Date: Thursday, June 15, 2006	Sheet 44 of 48	

MODEL	DATE	Change Note	
TW3A		Page	Description
	B to 1223	Page 29	Change R472 to NI for SATA,install for PATA to solve sometimes ODD can't be detected and slow boot..
		Page 33	Add R481,R480 to solve WLAN LED light leakage.
		Page 3	Change R177 to install and pull low to set VGA clock to 100MHz.
		Page 19	Change R345 to install to solve back light can't enable.
		Page 29	Change R245 to NI for SATA,install for PATA.
		Page 14	Add R482,R483 for CRT/DVI option.
		Page 24	Change C645 to 10uF for LAN 1.2V per Marvell recommendation.
		Page 19	R377 to install,R362,R364,R365 to NI. (Set default to G72M)
		Page 30	3V_DVDD connect to +3VSUS to solve WOR.
	1223 to 1224	Page 32	Change MQ1,MQ2,MQ3,MQ4 to BA000420Z07 to solve MODEM low performance.
		Page 37	Delete short pad.
		Page 38	Delete short pad.PC92 change to install.
		Page 39	Delete short pad.
		Page 41	Delete short pad.
		Page 42	Delete short pad.PR45,PR150 change to 75K(CS37502FB04).
		Page 43	Delete short pad.
		Page 5	R19 change to NI for solving power-on shutdown.
		Page 34	HOLE,3,HOLE4,HOLE7,HOLE8 change to MBRW1003011.
		Page 40	PR110 change to CS+0158JL11.PR132 change to 24.9K.
		Page 37	PC34,PC113,PC114,PC129 change to CH733RM8831.
		Page 23	F1 change to DK100TPU028.
		Page 33	Q17 change to install for BT LED control.
		Page 34	Change CN4 footprint to "afn250-a2g1t-25p-l" for SMT issue.
		Page 26	Change CN1.4 connection to RF_LED.
		Page 33	Add NET RF_LED.
		Page 36	Delete NET TUCHLED.
		Page 31	Change C541,C546 to X7R for audio precision.
	1223 to 1226	Page 38	Change PC93,PD9,PC168 to install. Delete NET 10V.
		Page 41	Change NET 10V to +15V_SUS.
		Page 26	LED2,LED3 change to dual color type(cost down and unify brightness and color).
		Page 12	Reserve C784 on THERMTRIP for ESD.
		Page 35	Reserve R497,R498,R499 for TW2 PR.
		Page 33	Delete RP45,RP46,R210 for layout problem.
	1226 to 1227	Page 33	Change CN23 to Molex (same as SW1). Add CN31 PCIE latch.
		Page 44	Add EMI spring B1,B2,B3.
		Page 32	Install MC8,MC9 for EMI.
		Page 12	Change C459 TO 22pF for EMI.
		Page 31	R479,R281,R295 change to install for EMI.
	1227 to 1228	Page 44	Add B4,C785,C786,C787 for EMI.
		Page 19	Reserve R504,R505,R506,R507 for DVI EMI.
		Page 3	Change Y1 P/N to BG614318081(CL=20pF) for solving system time delay issue.
		Page 23	Change C694,C701,C703 to NI for signal quality.
		Page 36	RN2 change to 4.7K for IIC signal quality.
		Page 30	C528,C529 change to 1uF/10V X5R for audio precision.
		Page 35	Add L60~L66,C788~C793 for EMI.
	1227 to 1230	Page 26	Change CN9,CN12 P/N to DFHS04FRE80.
		Page 36	Delete D13, add R508,R509,Q34 for PR leakage current. R454 change to 100K.

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Change Note	3A
Date: Thursday, June 15, 2006	Sheet 45 of 48	

Change Note

MODEL	REV	Page	Description
TW3A			
	1230 to 0102	Page 38	PC173 change to 470uF.
		Page 39	PC66 change to install.
		Page 42	PR153 change to 20K.
		Page 41	PD7,PD21,PD22 change to CH501.
		Page 37	PD6,PD5 change to CH501.
		Page 42	PQ47 change to RQW180N03.
		Page 26	CN12,CN9 USB connector change to DIP type.
		Page 29	CN25 pin25,26 and CN24 pin47,48 disconnect to GND.
		Page 23	CN6 pin27,28 disconnect to GND.
		Page 34	SW1,SW2 P/N change to DHP00FC1G16.
		Page 36	Change R454 to 100K,R508,R509 to 10K.
	0102 to 0103	Page 4	R101,R97,Q11 change to install.
		Page 6,7,8,9,10,11	Change U32 P/N to AJSL8Z40T26.(945PM)
		Page 12,13,14,15	Change U36 P/N to AJSL8YB0T12.(ICH7M)
		Page 37	PR128 change to 3.9K.
	0103 to 0105	Page 45,46	Update change list.
		Page 27	Change J1 P/N to DFHS04FRE47.
		Page 35	Change CN15 to install and P/N to DFHS48FR001
		Page 44	Change B1,B2,B4 P/N to FDTW3002018.
		Page 36	U38 P/N change to AKE35ZAKK17.
		Page 42	PR45,PR150 P/N change to CS37502FB12.
	0105 to 0111	Page 30	Change C528,C529 to 2.2uF/6.3V for audio precision.
C1 TO C2	0111 to 0119	Page 19	Change R26 to 0 ohm and change connection to THERM_OVER#.
		Page 23	Q21 mirror vertical.
		Page 23	Add C794~C799, L67~L69 for EMI.
		Page 23	L46,L44,L42 change to 0 ohm. C700,C702,C705 change to NI for EMI.
		Page 32	Change MR5,MR6,MR,MR10 to 280ohm. Add MR11,MR12,MR13. Change MR8 to NI.
		Page 35	R17 change to install.
		Page 35	CN15.21,22 change to CRT_GND. Add R512 for EMI.
		Page 35	Change D1 to page23 and its connection and to NI.
		Page 41	PL14 P/N change to DC-38600001.
		Page 43	PQ59,PQ61,PQ36 P/N change to BAM44220002.
		Page 36	RN2 P/N change to CJ247084N25.
		Page 26	LED4 P/N change to BEBL0002Z62. LED1~3 P/N change to BEAB0013ZA1.
		Page 33	CN10 P/N change to DFHS26FR489.
	0119 to 0120	Page 14	Change R368 to install,R366 to NI to set w/ docking.
		Page 27	Change D7 to install to solve 7402 does not work.
		Page 19	Delete R410,R413,R417 for EMI layout.
		Page 23	Correct CN6 C1~C4 pin define.
		Page 23	Reserve Q37,Q38,RP56,R513,R514 for DVI disable when docking attach.
		Page 29	CN25 footprint change to "SATA-C16647-122A4-B-22P-R-V" for SMT issue.
C2 TO C3	0120 to 0209A	Page 25	LAN active/link LED change to +3VSUS.

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Change Note

MODEL	DATE	Page	Description
TW3A			
C2 to C3	0209 to 0222A	Page 23	**(1)** CN20 pin 12,15 change connect to DVI_DDCDAT,DVI_DDCCLK **(In C1 was connect to DDCCLK2,DDCDAT2)**
			(2) R150,R159,Q37,Q38,RP56 Change to install for DVI,CRT I2C,D1 change to NI
			(3) Change L67,L68,L69 P/N from CX8BB121002 to CX8BB470007
			(4) Change C794,C795,C796,C797,C798,C799 P/N from CH01806JB07 to CH01006JB08
		Page 27	**(1)** Change R208 pin1 contact to +3VRUN
			Change R208 P/N to CS31002JB28,C473 change to CH4102K1B03 ,D7 change to NI.
		Page 34	**(1)** RP47,RP48,RP49 change to CJ3100A8N21(meet Rohs)
		Page 42	**(1)** Change PR147 to NI
Production	0222A to 0407A	Page 26	**(1)** Change CN9,CN12 layout footprint to usb-020133mr004s566zl-c-h
		Page 31	**(1)** Change U21 layout footprint to QFN28-5X5-5-33P(add thermal Pad)
	0407A to 0510	Page 23	**(1)** Change C794~C796 to 6.8PF(CH-6816TB05)
			(2) Change C797~C799 to 33PF(CH03306JB04)
			(3) Change L67,L68,L69 to BLM18BA750SN1D,75 0.3A(CX8BA750006)
	0510 to 0523	Page 12	**(1)** Change R186 from CS03902JB21 to CX5LL241002 , C459 from CH02206GB02 to NI
		Page 19	**(1)** Change R504~R507 from CS11502FB21 to CH01006JB08
		Page 27	**(1)** Change EB1,EB2 from NI to DC09004A014 ,R286~R289 from CS00002JB38 to NI
		Page 30	**(1)** Change R477,R478 from CS03902JB21 to CX8LL241008,R279,R285 from CS00003J951 to CX8LL241008,
			L33 from CX221T05009 to CX8LL241008
			(2) Change R256 to CS02202JB22,C539 to CH02206GB02*R256 from NI to CS02202JB22,C539 from NI to CH02206GB02
		Page 31	**(1)** Change R268,R278 from CS03303J941 to CX8LL241008
			(2) Change C564 from NI to CH11006F909

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A. G72M to G72MV

1. change P/N to G72MV (AJ073000T14)
2. Set VGA core to 1.0V fix.
3. Change PCI_DEVID.

B. VRAM 128MB to 64MB

1.follow config table to set RAM_CFG.

2.Change VRAM P/N to HYNIX.

3.VRAMx2

C. LAN GIGA to 10/100.

1.Change LAN chip to 8038(AJ080380000).

2.Change Rset resistor.

3.Change transformer.

D. SATA to PATA

1.Set ODD to slave.

2.Set HDD to master.

3. Remove SATA conn.

4. Add PATA conn.

5. Change board ID to PATA.

6. Install resistor to connect ODD and HDD LED.

7. NI resistor of SATA LED.

E. docking to no docking.

1.Set board ID4 to low.

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